Magnetoresistive Random Access Memory (MRAM)

By James Daughton
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I. Introduction

In 1984 Drs. Arthur Pohm and Jim Daughton, both employed at that time by Honeywell, conceived of a new class of magnetoresistance memory devices which offered promise for high density, random access, nonvolatile memory. In 1989 Dr. Daughton left Honeywell to form Nonvolatile Electronics, Inc. having entered into a license agreement allowing him to sublicense Honeywell MRAM technology for commercial applications. Dr. Pohm, Dr. Daughton, and others at NVE continued to improve basic MRAM technology, and innovated new techniques which take advantage of revolutionary advances in magnetoresistive devices, namely giant magnetoresistance and spin dependent tunneling.

Today there is a tremendous potential for MRAM as a nonvolatile, solid state memory to replace flash memory and EEPROM where fast writing or high write endurance is required, and in the longer term as a general purpose read/write random access memory. NVE has a substantial patent portfolio containing 10 MRAM patents, and is willing to license these, along with 12 Honeywell MRAM patents, to companies interested in manufacturing MRAM. In addition, NVE is considering internal production of certain niche MRAM products over the next several years.

II. Background

The development of MRAM has been based on a number of significant ideas over the past 20 years, starting with Cross-tie Random Access Memory (CRAM), and continuing with new configurations using first Anisotropic Magnetoresistance (AMR) materials and then using higher sensitivity Giant Magnetoresistance (GMR) and Spin Dependent Tunneling (SDT) materials. A brief background on precursors to magnetoresistive random access memory (MRAM) is followed by a description of an early MRAM, and then descriptions of cell configurations with improved signal levels including MRAM cells with GMR materials, Pseudo-Spin Valve (PSV) cells, and cells using SDT structures.

Early magnetic random access memory (as opposed to serial memories like tape and disk) used the natural hysteresis of magnetic materials to store data ('1" or "0") by using two or more current carrying wires or straps. Magnetic elements were arrayed so that only ones which were to be written received a combination of magnetic fields above a write threshold, while the other elements in the array did not change storage state. A simple version of a 2-D writing scheme of this type is illustrated in Figure 1. Most of today's MRAM concepts still use this write technique.

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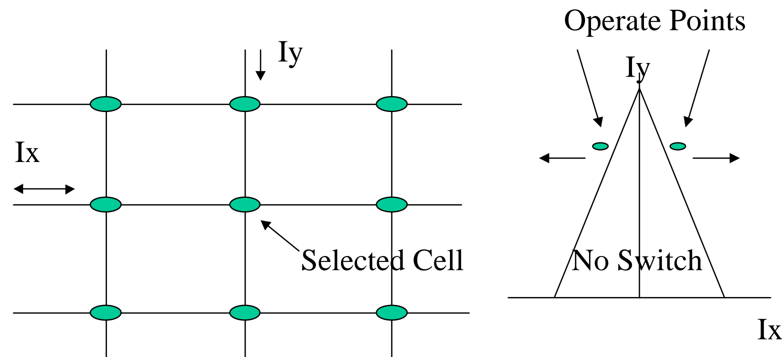


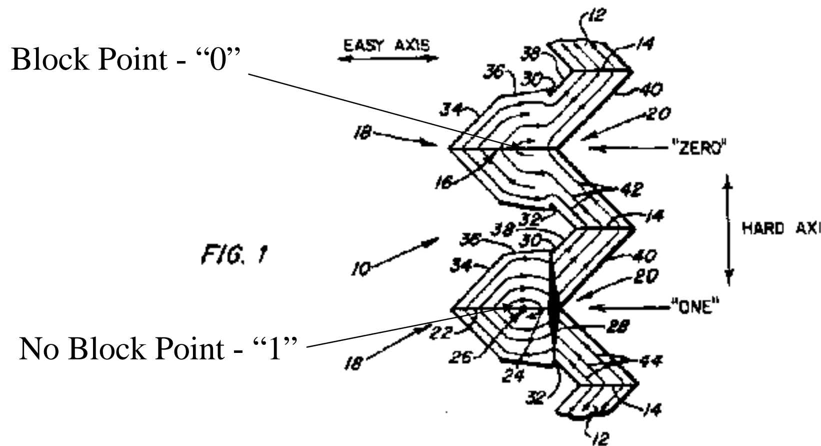
- Ix, Iy Alone Doesn't Switch Cell
- Ix, Iy Together Switch Cell

Figure 1. 2-D Magnetic Memory Cell Array And Selection Of Cell.

These early memories (mostly magnetic core memories) used inductive signals for determining the storage state ("1" or "0"). A magnetic field (current) was used to "interrogate" the memory element, and the polarity of induced voltages in a sensing circuit depended on whether a "1" or "0" was stored.

The first to propose a magneto-resistive readout scheme was Jack Raffel [1]. His scheme stored data in a magnetic body, which in turn produced a stray magnetic field that could be detected by a separate magnetoresistive sensing element. The concept was not high density because it was difficult to get a sufficiently large external stray field from a small magnetic storage cell. This scheme of separating the magnetic storage element from the sensor has similarity with the schemes recently proposed for magnetized bodies sensed by Hall effect sensors [2].

The first technology which used a magnetic element for storage and also used the same element for magnetoresistance readout was the Cross-tie



US Patent 5197025, L. Schwee and P. Hunter, “Crosstie Random Access Memory and a Process for the Fabrication Thereof” 1993

Figure 2. Crosstie Random Access Memory (CRAM)

Cell.Random Access Memory (CRAM) [3]. This cell used a slight difference in resistance of the cell depending on the presence or absence of a Block point to indicate a “1” or “0” as shown in Figure 2. There were difficulties in getting the cell to write consistently, and the difference in resistance between a “1” and “0” .was only about 0.1% of the inherent cell resistance, an impractically low signal.

The first published proposal for fabricating magnetic memory cells on a silicon support chip used inductive read-out rather than magnetoresistive readout [4]. This was (and still is) an important concept for MRAM because interconnections between an array of magnetic cells and the required circuitry to make a memory are probably too complex for separate memory and support circuitry.

III. Magnetoresistive Random Access Memory (MRAM)

In the mid 1980’s an MRAM concept was developed at Honeywell which has some common features with most modern versions.

- Writing using magnetic hysteresis
- Reading using magnetoresistance of the same body where data is stored
- Memory cells integrated on an integrated circuit chip

Figure 3 illustrates the method of data storage in the MRAM cell. The cell consisted of two ferromagnetic films sandwiching a poor conductor (TaN), with the composite film etched into stripes as shown. A current through the stripe

magnetized the NiFe clockwise or counterclockwise when aided by a current (field) from an orthogonal stripline. Current in either strip by itself would not change the storage state. Thus, a single memory cell could be selectively written in a 2D array [5].

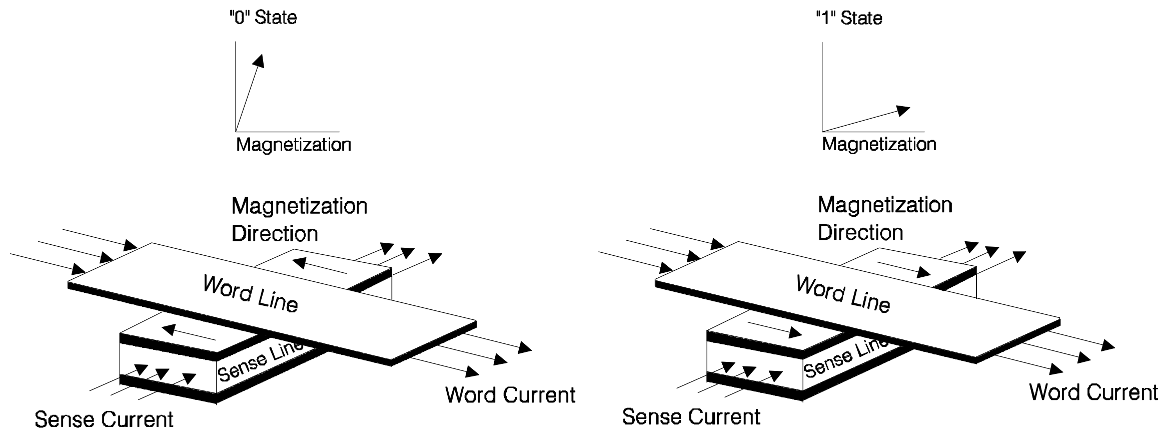


Figure 3. Earliest MRAM Concept.

Reading of this cell depended on the differential resistance of the cell when a sense current was passed through it. Because the sense current creates a magnetic field which opposes the magnetization in one storage state, but is in the same direction in the other state, the angle of rotation was different for a “1” or “0”. The magnetic material used was a cobalt-permalloy alloy with a normal anisotropic magnetoresistance (AMR) ratio of about 2%. Despite improvements in reading methods [6], the maximum differential resistance of the cell between a “1” and a “0” when it was read was about ¼ of the 2% magnetoresistance, or about 0.5%. In real arrays with practical sense currents, this gave differential sense signals of 0.5 to 1.0 mV. These sense signals allowed 16K bit integrated MRAM chips to operate with a read access time of about 250 ns [7]. Write times for the MRAM was 100 ns, and could have been faster if needed. A photomicrograph of a 256K bit MRAM chip produced by Honeywell is shown in Figure 4.

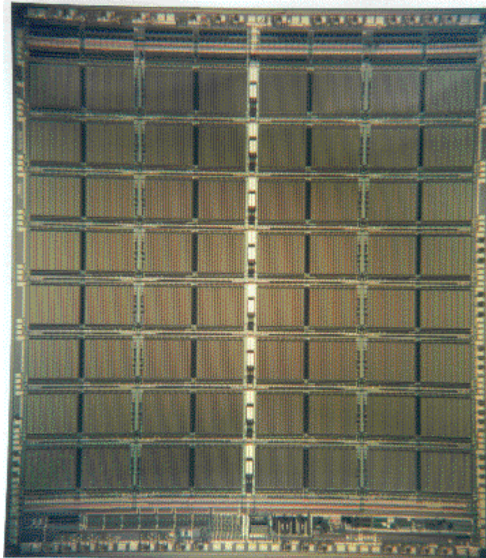


Figure 4. 256 K MRAM Chip (Courtesy of Honeywell).

The discovery of Giant Magnetoresistance (GMR) materials in 1989 [8,9] gave hope for higher signals and faster read access time. In 1991 magnetic films sandwiching a copper layer and etched into stripes showed a magnetoresistance ratio of about 6%. This magnetic configuration fit the aforementioned MRAM cell with little modification. Since the read access times tends to improve as the square of the signal, normal scaling would indicate that the improvement of a factor of 3 in magnetoresistance would lead to a 9 times improvement in read access time. Read access times of under 50 ns were achieved for MRAM with GMR materials [10].

Even with GMR materials this cell had serious limitations. The competition – semiconductor memory – was still faster because of the low MRAM sense signal. Worse, there was a limit to the reduction of cell size because the cell would not work with sense lines narrower than about 1 micron. This was due to magnetization curling from the edges of the stripe, where the magnization is pinned along the stripe. Due to exchange, there are limits to how quickly the magnetization can change directions with distance, and near the center of a 1 micron stripe, the magnetizations of the two magnetic layers in the sandwich would be directed substantially along the stripe, thus storing data very marginally.

IV. Pseudo-Spin Valve (PSV)

The invention of the Pseudo-Spin Valve (PSV) cell [11] significantly improved signal levels, thus improving the read access time of MRAM while maintaining

densities competitive with other solid state memory technologies. Not only was nearly all of the (approximately) 6% GMR available, but also the signal swing was plus or minus 6%, making the difference between a "0" and "1" about 12% of the cell resistance. This gave an 8 times improvement over the original mode of operation, and put MRAM on a much more even footing with semiconductor memory for read access time.

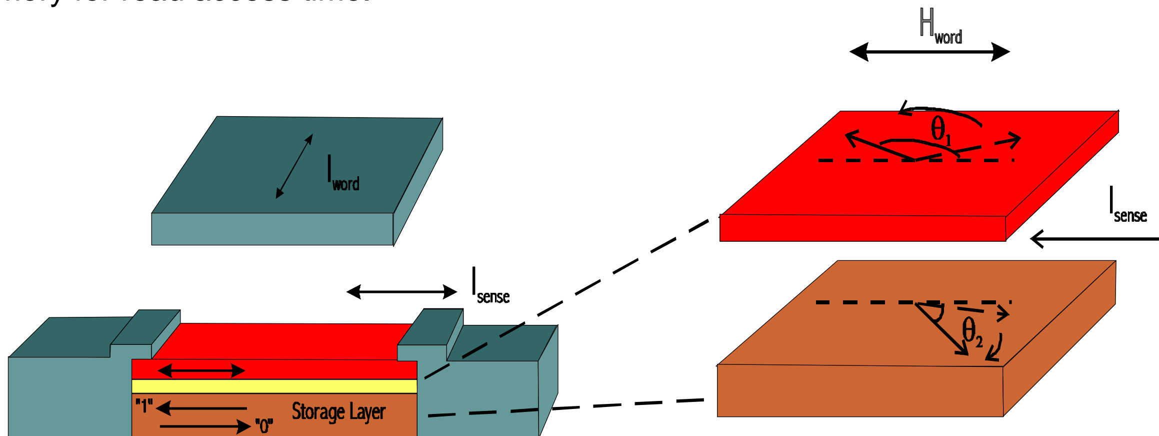


Figure 5. Pseudo-Spin Valve Cell.

Figure 5 illustrates the construction of a PSV cell. There are two magnetic layers that have mismatched properties so that one tends to switch at lower fields than the other. This can be done by using two magnetic films of the same material, but with different thicknesses. In that case, the thinner film switches at lower fields, or is the "soft" film and the thicker film switches at a higher field, and is the "hard" film. The resistance is lowest at the fields where the hard film switches to align with the soft film. The soft film acts as a means of reading the storage state, which is stored in the hard film. Without switching the hard film, the soft film can be manipulated to be parallel or antiparallel to the hard film. As shown in Figure 6, with a sequence of word fields which starts with a negative field and ends with a positive field, the resistance either rises or falls, depending on whether a "1" or a "0" is stored. With simple electronics, the difference between the initial and final resistances can be sensed, and the polarity of this difference indicates whether a "1" or "0" is stored.

PSV memory cells can be as narrow as 0.2 microns [12], and perhaps narrower, and using a 2D memory organization, PSV memory is probably the densest of the proposed MRAM schemes. The reported fields (currents) required to switch the hard layer have been too high to date for high density integrated circuits. PSV memory may find initial applications as a replacement for EEPROM or flash memory when high density or fast writing is important.

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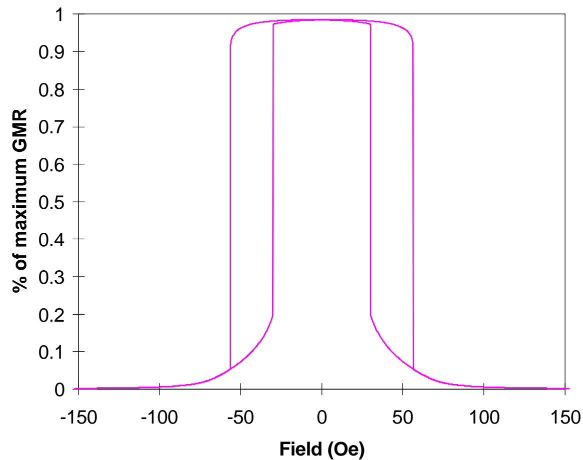


Figure 6. Pseudo-Spin Valve Resistance vs Magnetic Field Characteristic.

V. Spin Dependent Tunneling (SDT) Memory

Spin Dependent Tunneling (SDT) devices provides higher percentage magnetoresistance than sandwich or PSV structures, and thus has the potential for higher signals and higher speed. Recent results indicate SDT tunneling giving over 40% magnetoresistance [13,14] compared to 6-9 % magnetoresistance in good PSV cells.

(3X3 Xistor/Cell Array)

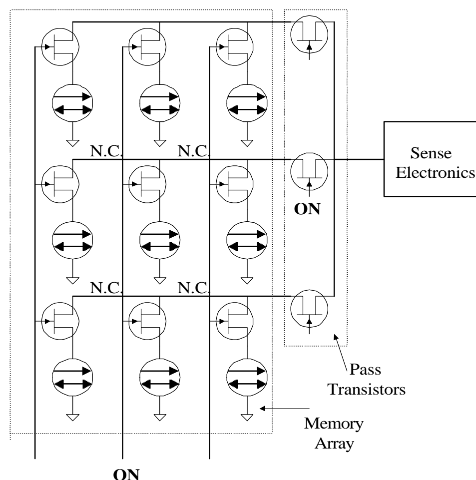


Figure 7. 3x3 Array of SDT Memory Cells.

The physical and magnetic similarities between magnetic sandwiches with copper interlayers and SDT magnetic sandwiches with dielectric interlayers suggests that SDT memory cells can be constructed in much the same fashion as PSV cells [15]. This is true with some limitations. The resistance of small tunneling cells tend to be at least several 1000's of Ohms, and they are subject to dielectric breakdown at the 1V to 2V level. Thus, currents of more than about 1 mA through the devices is not practical, and the currents used to sense the state of the SDT cell probably cannot be used to aid in the switching of the cell, unlike PSV cells. This suggests extra contacts and lower density for the SDT than for the PSV cell. Although there are also some time constant limitations for PSV cells, recent data [13] on lower resistance indicates that this problem can be overcome. The intrinsic speed of SDT elements configured into a DRAM type architecture (see Figure 7) or a flip-flop like cell (see Figure 8) should provide signals of 30-40 mV, which is comparable to semiconductor memory cells signal levels, and should thus run at comparable speeds. SDT memory show promise for high performance nonvolatile applications, including embedded latches for reconfigurable computing.

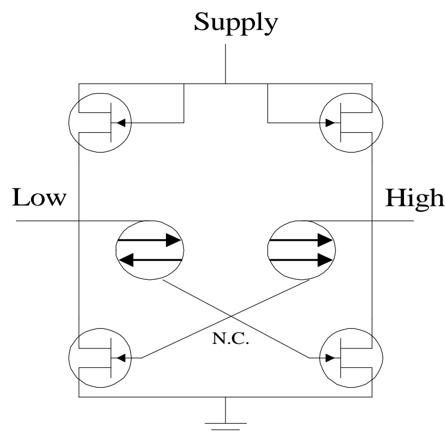


Figure 8. SDT Static RAM Cell

VI. Current Status

Several large companies currently have R&D programs on MRAM technology, and Honeywell has announced working MRAM components. With numerous competitors in the field, there has been a reluctance to publish results. But it is clear that MRAM has the potential to be as fast and dense as DRAM with the additional advantage of nonvolatility. Compared with flash and EEPROMs, MRAM writes much faster and does not deteriorate with millions of write cycles.

Ferroelectric RAM (FRAM) is like MRAM in that it is nonvolatile and fast write, and there has been some limited commercial applications. While FRAM is a competitor to MRAM, it is likely that MRAM can be denser, and thus less expensive.

VII. Challenges

Present day challenges for MRAM technology include 1) reducing drive currents, 2) eliminating cell instabilities due to magnetization vortices, 3) improving modes of operation at nanometer dimensions to avoid fundamental thermal instabilities, and 4) finding applications with sufficient volumes and performance advantages to make MRAM manufacturing costs competitive.

To be practical, dense MRAM cells should operate with less than a few mA currents when the lithography is at the 0.2 – 0.3 micron dimensions. Two reasons are: to stay within the current carrying capability of thin, narrow metal lines, and to be compatible with the center-to-center circuit spacing at the edge of the magnetic array. Reported data shows more than 10 times the desired current densities. Several mitigating ideas have emerged. One is to coat or "keeper" the tops and edges of the strip lines used in the memory array as shown in Figure 9. This has been shown to reduce word currents by a factor of 3 in unpublished work at NVE (see Figure 10]. An additional idea is to reduce the rise time of pulses, which takes advantage of the gyro-magnetic nature of the magnetization. This technique has reduced the required drive currents by a factor of more than 2 as shown in Figure 11 [16]. Devising methods whereby required current levels scale down with size of the memory cell will continue to be a challenge for MRAM.

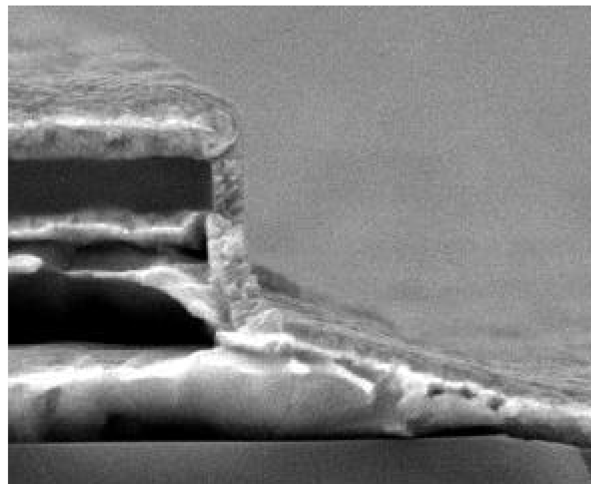


Figure 9. Cross-Section of "Keepered" Word Line (intermediate process step)

In the 1980's it was believed that as the memory cells approached the dimensions of a domain wall width, there would be no more problems with multi-domain magnetization in the cells, i.e. the magnetization would act as a single collection of spins with only one rest state. This myth was shown to be false by both experiment and data. Anomolies called "vortices" can occur in cells as small as a few tenths of a micron in diameter [17], and example of which is illustrated in a simulation shown in Figure 12. These can be prevented in PSV cells by using sharp ends [16], one example of which is shown in Figure 13, but at the expense of cell area. Recently, a circumferential magnetization storage mode in round MRAM cells has been proposed [18]. Vortices are the unanticipated problem in MRAM technology.

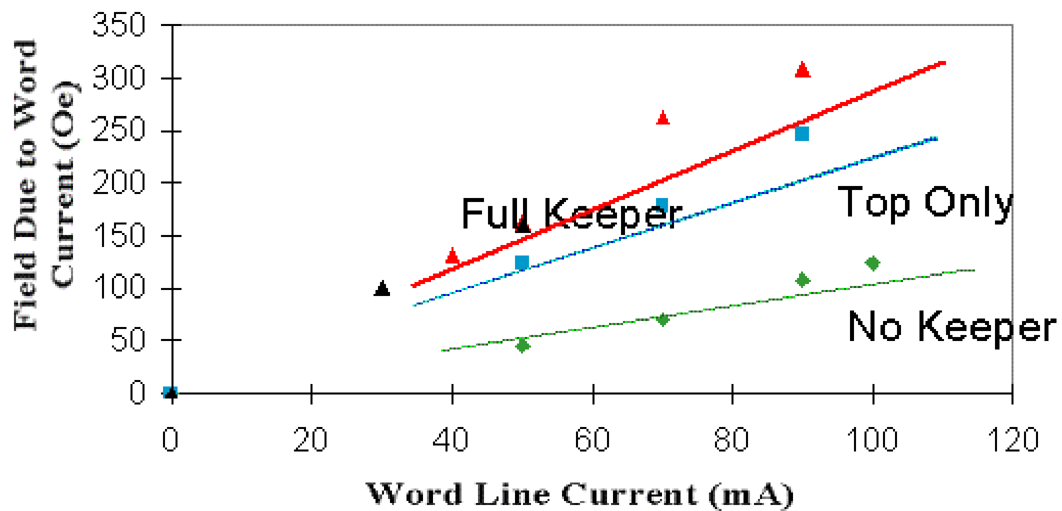


Figure 10. Field Enhancement Due To Keepers.

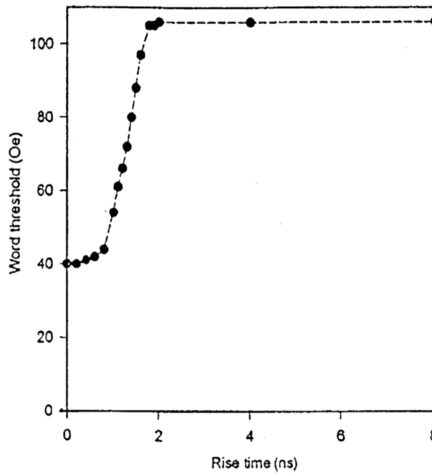
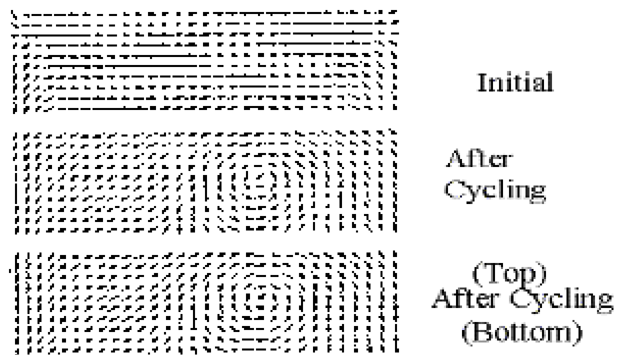


Figure 11. Word Field Required For Switching vs Rise Time.



J-G Zhu and Y. Zheng, Characteristics of AP Bias in Spin Valve Memory Elements", IEEE Trans. Mag. 1998

Figure 12. Simulated Spin Valve Memory Cell Anomaly.

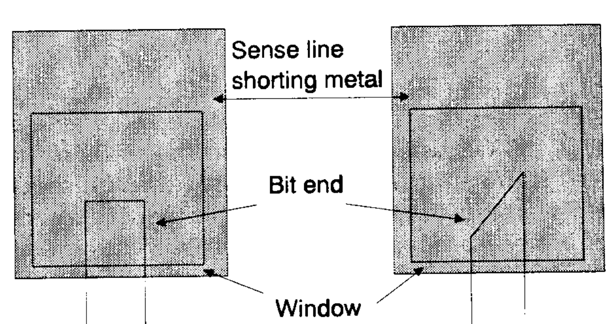


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Figure 13. Sharp Bit Ends For Improving PSV Stability.

The stability of the MRAM cell can be looked at as an energy well problem, where the energy associated with storage is MHcV, where Hc is a critical field which prevents magnetization reversal, M is the saturation magnetization, and V is the volume of the magnetic material in the cell. As the volume is reduced, the ratio approaches some multiple of kT (about 20) at which the error rate in the memory becomes unacceptable. Making Hc ever higher does not work because of the current required to write and the resultant heating of the cell (raising kT). With the present modes of operating, the practical lower limit to MRAM storage area would be about 0.1 micron on a side. A new idea is to use heat to help select the cell for writing and use the Curie point of an antiferromagnet to enable writing with a low current. Then at cooler temperatures, the energy well can be very deep. This is an idea that NVE is working on actively.

The last challenge is getting MRAM into high production levels. It requires investment, and a lot of it, perhaps as much as a billion dollars. It will take commitment from one or more companies to manufacture MRAM in high volume, in order to realize the tremendous potential of MRAM as a mainstream nonvolatile memory technology, but with the right investment, MRAM can be a very important mainstream memory technology.

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