SEEQ
Technology Incorporated

80C04A

AutoDUPLEX™ CMOS Ethernet Data Link Controller

PRELIMINARY *March 1994*

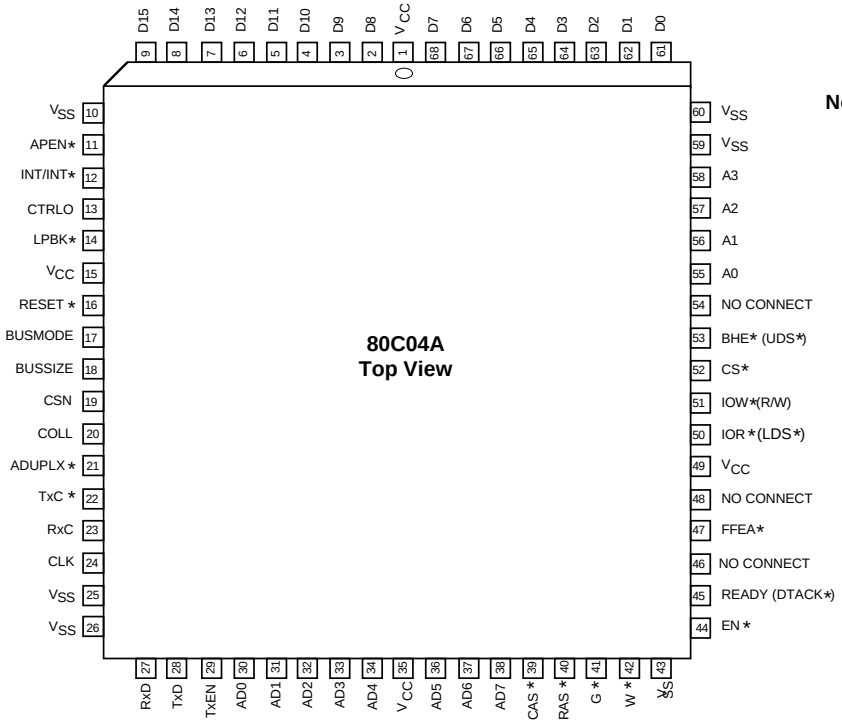
Features

- ***Pinout and function compatible with the 80C04 except for the function of bits 3 through 6 of the Transmit Packet Status Byte.***
- ***Following new features not available in the 80C04***
  - ***2nd Station Address Register available.***
  - ***Programmable bit to enable use of the hash table for filtering addresses other than multicast addresses.***
  - ***16 bit FCS (frame check sequence) error counter.***
  - ***16 bit short frame error counter.***
  - ***16 bit dribble frame error counter.***
  - ***8 bit oversized frame error counter.***
  - ***4 bit excessive deferral error counter.***
  - ***4 bit late collision error counter.***
  - ***4 new Transmit Packet Status bits indicating following transmit packet status conditions:***
    - ***Transmit okay but single collision occurred.***
    - ***Transmit okay but multiple collision occurred.***
    - ***Transmit okay but deferred.***
    - ***Carrier sense drop out during transmission.***
- ***Capable of operating with 40Mhz master clock frequency.***
- ***Conforms to IEEE 802.3 standard for Ethernet (10BASE5), Cheapernet (10BASE2) and Twisted Pair (10BASE-T).***

Note: Check for latest Data Sheet revision before starting any designs.

Call SEEQ Technology (510) 226-7400 x3051.

Pin Configuration



Note: Signal names in paranthesis apply when BUSMODE = 0

Note: Contact SEEQ for the latest Design Guide.

AutoDUPLEX is a trademark of SEEQ Technology Inc.

- ***High performance, low power CMOS technology.***
- ***Connects directly to 8020 and 8023 Manchester Converters (MCC™).***
- ***Pin and function compatible with the 8005 Advanced Ethernet Data Link Controller (AEDLC™).***
- ***Fast bus cycle to support 16-bit, 12Mhz ISA bus architecture.***
- ***Manages 64K bytes of Local Packet Buffer.***
  - ***Connects to RAS/CAS/Data/Control of 64K x 4 DRAMs.***
  - ***Automatic DRAM refresh.***
  - ***Supports Packet Chaining and Easy Transmit and Receive Error Handling.***
  - ***Automatic Padding of transmit packets to 64 bytes minimum packet size.***
- ***Hash Function and Table for multicast address filtering.***
- ***Flexible System Bus Interface.***
  - ***8 or 16 Bit data transfers with Byte Swap Capability.***
  - ***Selectable for Intel or Motorola Compatible Bus Signals.***
- ***Group address packet reception.***
- ***Sleep mode to conserve power when not in use.***
- ***Uses Fewer Support Chips***
  - ***Lower Systems Cost***
  - ***Higher Reliability***
- ***68-pin surface mount plastic leaded chip carrier package.***
- ***Supports AutoDUPLEX mode for Automatic full duplex operation, provides 20 MBits/sec bandwidth for switched networks.***
- ***Product I.D. Register.***

Pin Descriptions

An asterisk after a signal name signifies an active low signal. Parentheses around signal names indicate alternate BUSMODE pin functions, for example BHE(UDS*), BHE* is active when BUSMODE = 1 (Intel bus configuration), and (UDS*) is active when BUSMODE = 0 (Motorola bus configuration).*

Pin Number	Bus Interface
47	***FFEA*:*** *FULL FEATURE: When set low this pin enables the new bus interface features of the 80C04A. These include the use of the UDS* and LDS* strobes in Motorola mode and the BHE strobe in intel mode. When set high or left unconnected the bus interface is SEEQ 8005 compatible and pin 53 is ignored. This pin has an internal 35K ohm pull-up resistor.*
17	***BUSMODE:*** *An input which selects Intel-compatible bus signals when high or Motorola-compatible bus signals when low. This pin has an internal 35K ohm pull-up resistor.*
18	***BUSSIZE:*** *An input that selects the 8-bit system bus when low or 16-bit system bus when high. This pin has an internal 35K ohm mini mum pull-up.*
52	***CS*:*** *Chip Select, an input used to access the Packet Buffer and/or internal registers.*
55-58	***A0-A3:*** *Address inputs select internal registers for reading or writing. A0 selects high byte or low byte of a register in Full Feature Mode for Bus Mode = 1 (Intel Bus Mode), see Tables 1, 2 and 3, (pages 16, and 19).*
2-9 61-68	***D0-D15:*** *A 16 bit bidirectional system data bus. If BUSSIZE = 0, the bus is configured as 8 bits and D8-D15 are not used for data transfer. Byte order for Packet Buffer data transfers on a 16 bit bus is software configured by the Byte Swap Bit on Config Register #2, bit 0. Pins D8-D15 are also used to provide address information to the optional external Auxiliary PROM in both 8 and 16-bit modes.*
12	***INT(INT*):*** *When BUSMODE = 1, this is a high active interrupt output; when BUSMODE = 0 this output is low active.*
45	***READY(DTACK*):*** *A three-state output that indicates readiness to transfer data. When BUSMODE = 1, this output functions as a READY pin (Intel compatible); when BUSMODE = 0 this output is DTACK* (Motorola compatible). Refer to Tables 1, 3 (pages 16, 19) for bus control logic summary descriptions.*
44	***EN*:*** *An output used to enable external bi-directional three-state bus drivers, such as the 74LS245.*

Pin Number	Bus Interface
54	**N.C.:** No Connect.
46	**N.C.:** No Connect.
48	**N.C.:** No Connect.
53	**BHE* (UDS*):** BHE* when BUSMODE = 1, (Intel Bus Mode) and UDS when BUSMODE = 0, (Motorola Bus Mode). **BHE*** input, Byte High Enable, together with A0, provides separate access to high and low bytes of the 16-bit registers, refer to Tables 1 & 2, (page 16). **UDS*** input, Upper Data Strobe. Data is transferred on the rising edge of UDS*, and allows access to the upper byte (D8-D15) of a register. Use LDS* and UDS* to write to both upper and lower bytes simultaneously (16-bit mode only). This pin has an internal 35K ohm pull up resistor.
50	**IOR*(LDS*):** IOR* when BUSMODE = 1; LDS* when BUSMODE = 0. **IOR*** input defines the current cycle as a read, and provides transfer control on its rising edge. **LDS*** input, Lower Data Strobe, enables you to read or write to the lower data byte of a register (D0-D7), refer to Tables 2 & 5. Data is transferred on the rising edge of LDS*.
51	**IOW*(R/W):** If BUSMODE = 1, this input defines the current bus cycle as a write, and data is transferred on the rising edge of IOW*. If BUSMODE = 0, this input defines the bus cycle as a read if IOW* = 1 or write if IOW* = 0.
13	**CTRLO:** Control/Output, a general purpose control pin, level follows bit 12 of Configuration Register #2.

Pin Number	Network Interface
21	**ADUPLX*:** A active low input used to set the 80C04A into AutoDUPLEX Mode. In this mode the transmitter will not defer to active carrier sense signal. This pin has an internal 35K ohm pull-up resistor.
29	**TxEN:** An output to the Manchester Code Converter that enables transmission.
22	**TxC*:** An input from the Manchester Code Converter that is used to synchronize transmitted data.
28	**TxD:** The transmit data output to the Manchester Code Converter.
20	**COLL:** The collision detect input from the Manchester Code Converter.
19	**CSN:** The carrier sense input from the Manchester Code Converter.
23	**RxC:** An input from the Manchester Code Converter used to synchronize received data.
27	**RxD:** The receive data input from the Manchester Code Converter.
14	**LPBK*:** The Loopback control output. The pin level is complement of the Loopback Bit on Config Register #2 bit 11.

Pin Number	DRAM Interface
31-34 36-38	**AD0-AD7:** DRAM Packet Buffer address/data pins.
42	**W*:** An output to the DRAM buffer that enables a write.
41	**G*:** An output to the DRAM buffer that enables the DRAM's output drivers.
39	**CAS*:** An output to the DRAM Buffer that latches the Column Address of the DRAM.
40	**RAS*:** An output to the DRAM Buffer that strobes in the Row Address of the DRAM.

Pin Number	Miscellaneous
24	**CLK:** 20-40 MHz master clock input.
16	**RESET*:** Active Low reset Input. A low pulse on RESET* clears all configuration registers and pointer registers to 00. Following deassertion of RESET*, (i.e. the highgoing edge of the RESET* pulse), a wait of 4 microseconds is necessary before accessing the part. RESET* has an internal 35K ohm minimum pull-up.
11	**APEN*:** Active low Auxiliary PROM enable output.
1, 15, 35, 49	**V_{cc}:** Power Supply
10, 25, 26, 43, 59, 60	**V_{ss}:** Ground

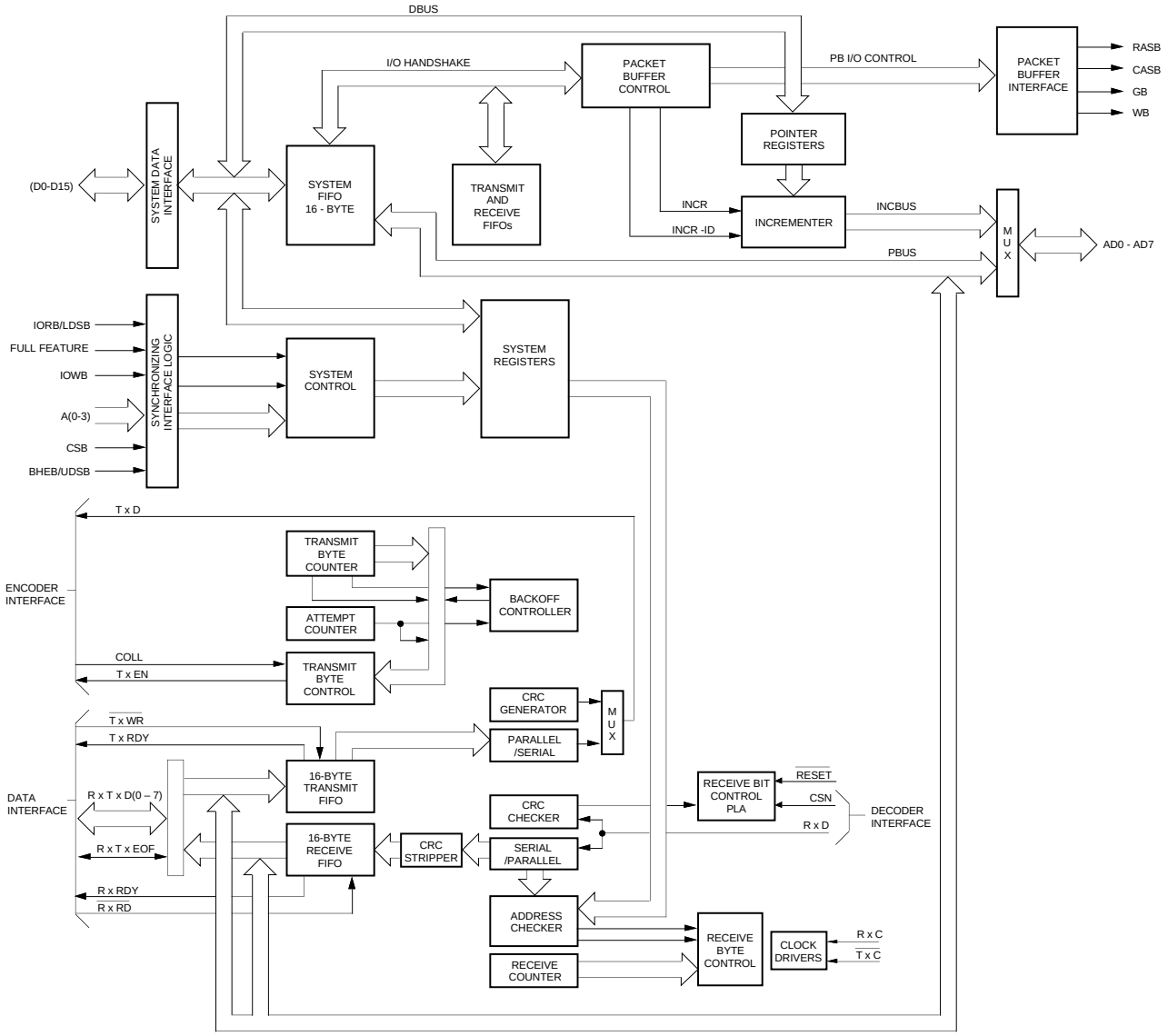
DESCRIPTION

The 80C04A has three major blocks: the Ethernet Data Link Controller, Buffer Controller, and Bus Interface.

The Ethernet Data Link Controller block supports the link layer (Layer 2) of the IEEE 802.3 standard. It performs serialization and deserialization, preamble generation and stripping, CRC generation and stripping, transmission deferral, collision handling, and multicast and broadcast addressing.

The Buffer Controller block provides management for a 64K byte local packet buffer consisting of two 64K x 4 DRAMs. This block provides arbitration and control for four memory ports: the transmitter, for network transmit packets; the receiver, for received frames; the Bus Interface, for system data and control; and an internal DRAM refresh generator. To minimize the pin count, dynamic RAM addresses and data are time multiplexed on a single 8-bit bus. A control line and 8-bit address is also provided to

80C04A Internal Functional Block Diagram



permit reading from a locally attached EEPROM or PROM. This permits configuration of an adapter board with its station address and configuration data, independent of the network layer software used.

The Buffer Controller interfaces to the system bus via the Bus Interface block and provides access to internal configuration and status registers, the local packet buffer and a control signal interface to permit programmed I/O transfer of packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called the System FIFO. This permits high speed data transfers to occur even when the Buffer Controller is busy servicing the transmitter or receiver or refreshing the DRAM. Both 8 and 16 bit transfers are supported. Byte ordering on a 16 bit bus is available under software control. The 80C04A supports both Intel-compatible and Motorola compatible buses.

The 80C04A Interconnect Diagram

The system interconnect diagram on page 7 shows the 80C04A in a typical system configuration, connecting to the LAN via an 8020 Manchester Code Converter. The Attachment Unit Interface connects to an Ethernet (10BASE-5); Cheapernet (10BASE-2) [83C92 Coaxial Transceiver]; or a twisted pair (10BASE-T) network 83C94 10BASE-T Transceiver.

Separate TMS 4464-120 64K DRAMs store received packets, or packets waiting for transmission. AD_0 -AD_7 address both RAMs. Data is exchanged on the AD leads, DQ_0 - DQ_3 to one RAM, and DQ_4 - DQ_7 to the other RAM.

The System Bus exchanges data with the Buffer Controller in the 80C04A. Two bi-directional data buffers (74LS45) interface 16-bit data, only one buffer is used for 8-bit data. The 2804 PROM stores the node address. The 80C04A has one 6-byte address field.

BUFFER MANAGEMENT

The Buffer Controller manages a 64K byte packet buffer into which packets that are received are temporarily stored until the system either reads or disposes of them and packets placed there by the system are held for transmission over the link. The buffer is logically divided into separate receive and transmit areas of selectable size. The transmit area always originates at address 0. Each packet in the buffer is prefixed by a header of 4 bytes that contains command and status information and a 16 bit pointer to the start of the next packet in the buffer.

To transmit packets, the system loads one or more packets of data, complete with header information, into the transmit area of the buffer and commands the 80C04A to begin transmission, starting from the address contained in the Transmit Pointer. When transmission is complete, the 80C04A updates the status byte in the header and interrupts the system if so programmed. The Transmit Pointer automatically wraps to location 0 when the Transmit End Area is reached.

The Buffer Controller manages the buffer area as a circular buffer with automatic wraparound. As data is received from the 80C04A it is stored in the buffer beginning at the location specified by the Receive Pointer. The Receive Pointer will wrap from FF, FF to Transmit End Area + 1,00. For example, if TEA = 80 the Receive Pointer wraps to 81, 00. If the Receive Pointer reaches Receive End Area, 00 an overflow has occurred. The Receiver is turned off and an interrupt is issued. Restarting the Receiver is accomplished by freeing up buffer space and turning the Receiver back on.

Transmit Packet Format

Each Packet to be transmitted consists of a four byte header and up to 65,532 bytes of data which are placed into the local buffer via the Bus Interface (page 17). The header contains the following information in the indicated order:

1. *Most significant byte of the address of the next packet header.*
2. *Least significant byte of the address of the next packet header.*
3. *A transmit command byte.*
4. *A transmit status byte which should be initialized to zero by the system and will contain status for this packet when transmission is complete.*

When reading the transmit packet header all four bytes must be read as a non-interruptable sequence. This is necessary to prevent the Bus Interface from interleaving writes to the packet header while the transmitter section is reading it.

Transmitter and Receiver sections will be able to run independently at different clock rates without impairing performance in other sections. TxC and RxC clocks can be operated independently at any speed between 1 Mhz and 10Mhz, without hanging up the rest of the system.

***Bytes 1 and 2,** called the Next Packet Pointer, point to the location immediately following the last byte of the packet, which is the first byte of the next packet header, if it exists. In 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB*

storage convention of the processor/bus being used. The byte order of the next packet pointer can be changed from MSB first to LSB first by setting bit #7 of configuration register #3 to a HIGH value.

***Byte 3** is the Transmit Command byte. It contains information to guide the controller in processing the packet associated with this block.*

***Bit 0: Xmit Babble Int. Enable.** The 80C04A will transmit packets as large as the Transmit buffer can hold but will abort packets and interrupt if this bit is set to a one. This condition is caused by an attempt to transmit a packet larger than the allowed 1514 bytes, excluding preamble and CRC. If babble occurs with bit 0-Xmit Babble Int. Enable set to a 1 on byte 3-the Transmit Command byte, the Transmitter will abort transmission and turn itself off. When the bit is set to 0, no interrupt is generated, and the Transmitter is not turned off, but a status bit is set in the Status Header.*

***Bit 1: Xmit Collision interrupt Enable.** When set to a one, a Transmit Interrupt will be generated if a collision occurs during a transmit attempt.*

***Bit 2: 16 Collisions Enable.** When set to a one, a Transmit Interrupt will be generated if 16 collisions occur during a transmit attempt, and the transmitter will be turned off. When set to 0 no interrupt is generated, and the transmitter will not be turned off, but a status bit is set in the Status Header.*

***Bit 3: Xmit Success Interrupt Enable.** When set to a one, a Transmit Interrupt will be generated if the transmission is successful, that is, fewer than 16 collisions occurred.*

***Bit 4: SQET Test Enable:** When set to a one and if bit 2 of configuration register 3 is set high, enables Signal Quality Error Test. Cleared to disable it. The test will occur or not occur on a packet-by-packet basis controlled by this bit. The test cannot fail if it is not enabled.*

Notes on SQE test sequence.

The transmitter of the 80C04A can be programmed to perform a Signal Quality Error Test, (SQE Test of Heartbeat Test), by writing bit 2 of configuration register 3, (indirect address = 1100), high. Once this bit is set, the test will occur or not occur on a packet-by-packet basis controlled by bit 4 of the Transmit Command byte. Bit 11 of the Status Register is the SQE Test Pass (status) bit. SQE Test Pass is set low if and only if there is an SQE Test failure. Whenever this bit is set low, if the Tx Int Enable bit is HIGH, the TX Int bit will also be set and an interrupt will be issued.

Once set low, it stays low until:

(1) Hardware Reset is asserted;
(2) Software Reset is asserted;
(3) The local processor writes a one to bit 6 of the Command Register 1, Tx Int Ack.

When an SQE Test failure occurs, the Transmitter is turned off automatically, and if transmit interrupts are enabled, an SQE Test failure will produce an interrupt and set the Tx Int Bit.

If the No Tx Fail Bit and/or the SQE Test Pass Bit is LOW the Transmitter will not turn on (it will be disabled). The local processor must clear the error bit by writing 1 to the Tx Int Ack Bit before turning on the Transmitter. This is to assure that the possibly serious error condition is noticed.

After a Transmitter shutdown due to an SQE Test failure, the Transmitter can be re-started by writing 1 first to the Tx Int Ack Bit and then to the Set Tx ON Bit. It will then continue with the next packet, if there is one, or again shut down if there is not.

SQE Test failure is defined as follows: Test begins when Carrier Sense is asserted (CSN goes HIGH). Test ends 4.0 to 4.4 microseconds after Carrier Sense is de-asserted (CSN goes Low).

Results are as follows: If during the course of the test at some time the local Transmitter was active, AND at no time was the Collision Signal asserted for more than 300 ns, then the test result is FAIL and the SQE Test Pass Bit gets set low. Otherwise the test does not fail.

***Bit 5: Data Follows:** If this bit is cleared to a zero, the transmitter will process this header as a pointer only, with no data associated with it. This provides a means to redirect the Transmit Pointer.*

***Bit 6: Chain Continue.** If set to a one, there are more headers in the chain to be processed. If this bit is a zero, the header is the last one in the chain.*

***Bit 7: Xmit/Receive.** If this bit is a one, the current header is for a packet to be transmitted. If this bit is a zero, the packet header will be processed as a header only and no data follows (bit 5).*

***Byte 4** is the Transmit Status byte, which is written by the Buffer Controller upon conclusion of each packet transmission or retransmission attempt. It provides for reporting of both normal and error termination conditions of each transmission.*

Bit 0: Xmit Babble. *If set to a one, transmit babble occurred during the transmission attempt. This is caused by an attempt to transmit a packet larger than the allowed 1514 bytes, excluding preamble and CRC. If babble occurs with bit 0-Xmit Babble Int. Enable set to a 1 on byte 3, the Transmit Command byte, the transmitter will abort transmission and turn itself off.*

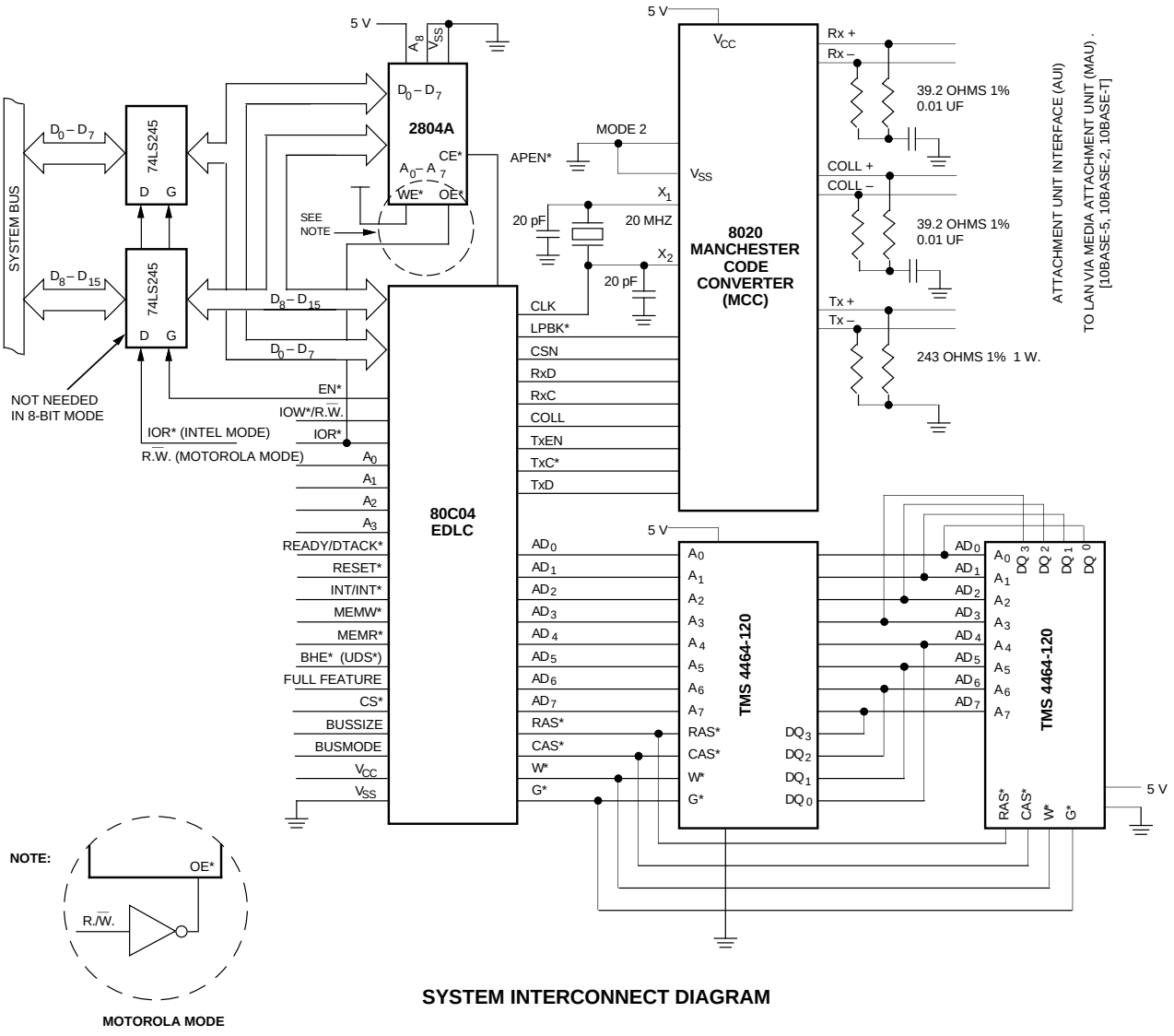
Bit 1: Xmit Collision. *If set to a one, a collision occurred during the transmission attempt.*

Bit 2: 16 Collisions. *If set to 1, 16 collisions occurred during the transmission attempt.*

Bit 3: Carrier Sense Dropout. *If set to a 1 carrier sense never went high or went from high to low during a transmission.*

Bit 4: Tx Okay but Deferred. *If set to a 1 the transmitter had to defer to carrier sense being high before transmitting a packet.*

Bit 5: Tx Okay but Multiple Collisions. *If set to a 1 the transmitter had to attempt transmission of a packet more than once but less than 16 times before completing transmission successfully.*



SYSTEM INTERCONNECT DIAGRAM

Bit 6: Tx Okay but One Collision. *If set to a 1 the transmitter had only one retransmission attempt of the packet before transmitting it successfully.*

Bit 7: Done. *If set to a one, the controller has completed all processing of the packet associated with this header (either the packet has been sent successfully or 16 collisions occurred) and there is now valid status in the Status byte.*

The data field follows the fourth byte.

Interpacket Gap Timer and Backoff Timer

The Transmitter will defer (postpone transmission) under the following conditions: Carrier Sense being HIGH, the Interpacket Gap (IPG) Timer is running, and/or the Backoff Timer is running. The timers are said to be running if they have started timing and the interval has not yet expired. If they are not running they are either expired or reset, and will not cause deference in these states. Following the 802.3 specification, the minimum defer time is divided into two periods. During the 1st two thirds period of defer time, detecting a carrier sense HIGH condition will cause the IPG counter to be reset to 0 until carrier sense is detected LOW. During the last one third of the defer time, the transmitter ignores carrier sense and, if it is ready to transmit a packet, begins transmission even if carrier sense goes HIGH.

If a collision with the local node occurs, the local node, within one byte time of seeing the collision signal COLL HIGH, ends normal transmission and begins transmitting the 'Jam' pattern, four bytes of all ones. The Jam reinforces (lengthens) the collision to assure all nodes can detect the collision. Upon completion of the Jam, the Transmitter returns to the IDLE state and starts the Backoff Timer. The Backoff Timer runs independently of the IPG Timer. After a collision, both timers will run, the Backoff Timer starting at the end of Jam, and the IPG timer starting at the de-assertion of Carrier Sense (CSN going LOW).

Both the IPG Timers and the Backoff Timer must be not running to enable the 80C04A to begin to transmit. When a packet becomes available to transmit, if Carrier Sense is inactive (CSN is low) and the timers are not running, the transmission will begin immediately. Once transmission begins, only a collision will cause the Transmitter to discontinue transmission of the packet before the end is reached.

If the 80C04A is in full-duplex mode ADUPLX asserted 'low' (pin 46), the IPG timer starts from the de-assertion of transmit enable (TXEN going low). When a packet becomes ready to transmit, the value of carrier sense is ignored and transmission will begin after the IPG interval even if carrier sense is high.*

Transmit Packet Chaining

Bits 6 and 5 of the Transmit Header Command byte control transmit packet chaining. They should be read together as follows (page 17, Byte #3 of Transmit Header):

Chain Continue (Bit 6)	***Data Follows (Bit 5)***	
1	*1*	*- Transmitter sends appended packet, then goes on to next packet.*
0	*1*	*- Transmitter sends appended packet, then turns OFF.*
1	*0*	*- Skip Header: Transmitter skips current packet, goes on to next packet using Next Packet Pointer.*
0	*0*	*- Null Header: Transmitter turns OFF without sending packet.*

These two bits are the only control bits required for transmit packet chaining. Bits 5 and 7 can be interchanged in the above table.

Note that the Skip Header can be used to relocate the Transmit Pointer to the beginning of another packet chain.

Note that the Chain Continue Bit of the last packet in a chain can be used to terminate a packet chain. Alternatively, placing a NULL HEADER following the last packet of a chain can also be used to terminate the chain.

To add to a packet chain while the transmitter is transmitting the chain, the following procedure is recommended:

a) Set Chain Continue = 1, Data Follows = 1, and Xmit/Receive = 1 on all packet headers that have data to transmit.

b) Before starting the Transmitter, write a Null Header (4 bytes of zeros) immediately following the last packet in the chain.

c) Start the Transmitter.

d) To add packet(s) to the chain.

1. *Write the next packet data immediately following the Null Header.*
2. *Optional: Write one or more complete packets with complete headers following the one in step 1.*
3. *Write another Null Header following the new packet(s).*
4. *(Last) Over-write the first Null Header with the correct header data for the packet.*

If the Transmitter catches up, it will stop at the first Null Header and, if Tx Int Enable is 1, will generate an interrupt. It will not "de-rail" or misread a header if the headers are written in natural order.

RECEIVE PACKET FORMAT

Each Packet received is preceded by a four byte header and is placed into the local buffer via the Buffer Controller. The header contains the following information in the indicated order:

1. *Most significant byte of the address of the next packet header.*
2. *Least significant byte of the address of the next packet header.*
3. *Header Status byte.*
4. *Packet Status byte .*

Bytes 1 and 2, *called the Next Packet Pointer, point to the first byte of the next receive packet header. The next packet header starts immediately after the end of the current packet. The packet length is equal to the difference between the starting addresses of the two packet headers minus 4. If the value of the Next Packet Pointer is less than the current one, the pointer has wrapped around from the end of the buffer to the Receive Start Area (the Receive Start Area equals the Transmit End Area address + 1). When in 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used.*

The third byte *of the header contains header information associated with this packet.*

Bits 0 through 5: *Not Used.*

Bit 6: Chain Continue. *If this bit is set to a one, there are more packets in this chain to be processed. If this bit is a zero, this packet is the last one in the chain and this header space will be used for the next packet that is received.*

Bit 7: Xmit/Receive. *This bit is always set to 0 by the controller to indicate a receive packet header.*

The fourth byte of the *header, called the Packet Status byte, contains status information resulting from processing the packet associated with this block.*

Bit 0: Oversize Packet. *If this bit is a one, the packet was larger than 1514 bytes, excluding the Preamble and CRC fields.*

Bit 1: CRC Error. *If this bit is a one, a CRC Error occurred in this frame.*

Bit 2: Dribble Error. *Packets are integral multiples of octets (bytes). If this bit is a one, the received packet did not end on an octet (byte) boundary.*

Bit 3: Short Packet. *If this bit is a one, the packet contained less than 64 bytes including CRC. Short packets are properly received as long as they are at least 6 bytes long; packets with less than 6 bytes will only be received if the match mode bits in Configuration Register #1 specify promiscuous mode, or multicast/broadcast is selected and the first bit of the destination address is a 1.*

Bits 4 , 5 and 6: *Not used.*

Bit 7: Done. *If this bit is a one, the controller has completed all processing of this packet and there are now valid pointers and status in this header. The user may now move this packet out of the local buffer, if desired, and reuse this buffer space.*

The data field follows this byte, unless this is a header only packet.

Interrupt Events, Automatic Transfer/Receiver Turn Offs and Special Conditions

The following summarizes the behavior of the transmitter and receiver sections following an event which generates an interrupt and other special conditions.

Events Which Generate Transmit Interrupts.

(Note: Refer to the Status Register (read only). All events listed here will set the Tx Int bit HIGH. These events will generate an interrupt if and only if the Tx Int Enable bit is set HIGH.)

a) Packet transmitted successfully and Tx Success Enable bit is HIGH in the packet header.

b) Packet transmitted successfully and the packet is the last packet in the chain.

(Note: Following this event the Transmitter will turn off automatically. To resume packet transmission, the local processor must turn it back on.)

c) SQE Test Enable bit is set and SQE test fails.

(Notes: 1. This event will set the SQE Test Pass Bit LOW (Status Register), whether the Tx Int Enable Bit is HIGH or not.

2. Following this event, the Transmitter will turn off automatically. To resume packet transmission, the local processor must turn it back on.)

d) Sixteen consecutive collisions has occurred and sixteen Collisions Enabled Bit is HIGH.

(Notes: 1. This event will set the No Tx Fail Bit LOW (Status Register), whether the Tx Int Enable Bit is HIGH or not.

2. The transmitter will turn off automatically if the packet is at the end of chain. If this is not the last packet in the chain, (i.e. bit 6 of the command byte for the packet header is high), transmission will continue with the next packet in the chain.)

e) The 1514th byte of a packet (including address fields, length field and data field) has been transmitted and that is not the last byte, and the Babble Enable Bit is set HIGH.

f) A single collision has occurred and the Collision Enable bit is HIGH.

g) Bits 10 & 13 of the Command Register are written high, at the same time.

Events which cause the Transmitter to Automatically Turn Off.

a. Transmitter finished processing the last packet in a chain.

b. Transmitter has a Babble Error and Babble Int Enable is set HIGH in the packet header.

c. Transmitter has an SQE Test failure (which can only happen if the test in enabled).

d. The local processor writes 1 to the Set Tx OFF Bit.

e. The chip is reset by either the RESET Pin or the Reset Bit.*

Events Which Generate Receive Interrupts

a) Receiving and storing an error-free packet in the Receive Buffer.

b) Receiving and storing an oversize packet in the Receive Buffer.

c) Receiving and storing a packet with Short Packet Error in the Receive Buffer (for this to occur, the Short Packet Enable Bit must be set High, otherwise a short packet will be discarded).

d) Receiving and storing a packet with Dribble Error in the Receive Buffer (for this to occur, the Dribble Error Enable Bit must be set HIGH, otherwise a dribble packet will be discarded).

e) Receiving and storing a packet with CRC Error in the Receive Buffer (for this to occur, the CRC Error Enable Bit must be set HIGH, otherwise a defective packet will be discarded).

f) The Receive Buffer overflows.

g) Bits 9 & 12 of the Command Register are written high at the same time.

(Note: All listed events above will set the Rx Int Bit HIGH and generate an interrupt if and only if the Rx Int Enable Bit is HIGH.)

Note: Receive Headers and Buffer Overflow

Upon receiving a packet, the Receiver will write a NULL HEADER (four bytes of zeros) in memory immediately after the packet data, then it will update the received packet's header with its Next packet Pointer and Status. All header write operations are non-interruptable sequences, to prevent the Bus FIFO from interleaving reads with writes of the same header.

A possible exception exists if there is a buffer overflow. In the event of Receiving Buffer overflow, the 80C04A will follow the last good packet with a NULL HEADER (four bytes of zeros) before shutting down. These bytes will not be written over data protected by the Write Protect Pointer. The exception: If there is not room to write a complete NULL HEADER after the last packet, the header preceding the last packet is not updated and remains a NULL HEADER, and the last packet is lost.

REGISTERS

There are nine directly accessible 16 bit registers in the 80C04A, one of which is used as a "window" into indirectly accessed registers as well as the local buffer memory. In non-fullfeature mode, access to the nine directly accessible 16-bit register are controlled by chip select, I/O read, I/O write and four address inputs, A0-A3. The following description assumes a 16 bit wide system interface in non-fullfeature mode. As such, the low order address input, A0, is shown as "X" a don't care. In 8-bit non-fullfeature mode, input pin A0 selects bits 0 through 7 of the register when a zero, and bits 8 through 15 when a one. A description of, how registers are accessed in fullfeature mode is given under the Full Feature Mode description later in this datasheet. Note that the byte swap bit does not affect the byte order of these registers.

All "not used" bits should be set to 0 to maintain future compatibility. When read, "not used" bits read as '0'.

Command Register, A3-0 = 000X (Write only)

Bit 0: Test Interrupt Enable. *If set to a one, enables a system producible interrupt.*

Bit 1: Rx Interrupt Enable. *When set to a 1, this bit enables interrupts whenever a packet becomes available in the packet buffer.*

Bit 2: Tx Interrupt Enable. *When set to a 1, this bit enables interrupts for completion of transmit operations. See the Transmit Header Command byte description for conditions that can cause an interrupt.*

Bit 3: Buffer Window Interrupt Enable. *Setting this bit to a one enables interrupts for Buffer Window register reads from the packet buffer.*

Bit 4: Test Interrupt Acknowledge. *Setting this bit to a one causes a pending test interrupt to be cleared.*

Bit 5: Rx Interrupt Acknowledge. *Setting this bit to a one causes a pending Receive interrupt to be cleared.*

Bit 6: Tx Interrupt Acknowledge. *Setting this bit to a one causes a pending Transmit interrupt to be cleared.*

Bit 7: Buffer Window Interrupt Acknowledge. *Setting this bit to a one causes a pending Buffer Window interrupt to be cleared.*

Bit 8: Set Test Interrupt. *Used to produce a system generated interrupt. Writing a one to this bit and bit 11 at the same time will generate an interrupt if bit 4 has been written to a one.*

Bit 9: Set Rx On. *Setting this bit to a one enables the Receiver. Clearing this bit to a 0 has no effect. Setting this bit with bit 12 set will force an interrupt, provided the Receive Interrupt Enable bit is set, which permits testing the interrupt without receiving packet data.*

Bit 10: Set Tx On. *Setting this bit to a 1 enables the Transmitter. The Buffer Controller will read the header information pointed to by the Transmit pointer and process the packet accordingly (see transmit packet header description). The conditions for interrupting upon completing packet processing are specified in the Transmit Header Command byte, which is stored in the buffer memory. Setting this bit with bit 13 set will force a transmit interrupt for test purposes.*

Bit 11: Set Test Interrupt. *Used to produce a system generated interrupt. Writing a one to this bit and bit 8 at the same time will generate an interrupt if bit 4 has been written to a one.*

Bit 12: Set Rx Off. *When Set Rx OFF is activated by writing 1 to bit 12 of Command Register 1, the Receiver will shut off immediately if not currently receiving, or after finishing the current packet if one is in process. The Rx ON Bit will remain HIGH while the Receiver is still receiving a packet. Interrupt will still be posted if appropriate, even after Set Rx OFF has been written HIGH. The interrupt is not set when Rx is turned off by the local processor unless there is another condition which warrants an interrupt. If RX Int Enable = 1, an interrupt will be generated when the Receive Buffer overflows. This condition also causes the Receiver to turn off automatically.*

(Note: When turning the receiver off, to insure proper operation of chip the receiver should be verified as being off by making sure bit 9 of the Status Register is HIGH, before attempting to turn the receiver back on again.)

Bit 13: Set Tx Off. *Setting this bit to a one disables the transmitter. If a packet is being transmitted when this bit is set, the packet will be aborted.*

Bit 14: FIFO Read. *When set to a one, the SYSTEM FIFO direction is set to read from the packet buffer. The FIFO direction should not be changed from a write to a read until it is empty (see FIFO status bits).*

Bit 15: FIFO Write. *When set to a one, the SYSTEM FIFO direction is set to write to the packet buffer. Changing the SYSTEM FIFO direction clears the SYSTEM FIFO.*

Status Register, A3-0=000X (Read only)

Bit 0: Test Interrupt Enable: *Same value and meaning as bit 0 of the Command Register.*

Bit 1: Rx Interrupt Enable. *When set, this bit indicates that interrupts are enabled for receive events.*

Bit 2: Tx Interrupt Enable. *When set, this bit indicates that interrupts are enabled for transmit events.*

Bit 3: Buffer Window Interrupt Enable. *When set, this bit indicates that interrupts are enabled for Buffer Window reads from the packet buffer.*

Bit 4: Test Interrupt Acknowledgment: *When set, this bit indicates that a system generated interrupt has occurred by writing bits 8 & 11 in the command register high at the same time. If the test interrupt enable bit is set, an interrupt is also asserted on the interrupt pin.*

Bit 5: Rx Interrupt. *When set, this bit indicates that a Receive packet chain is available. If the associated Interrupt Enable bit is set, an interrupt is also asserted.*

Bit 6: Tx Interrupt. *When set, this bit indicates that a Transmit interrupt condition has occurred. The following are valid Tx Interrupt conditions: Xmit Babble, Xmit Collisions, Xmit 16 Collisions, SQE test failure when the test is enabled, and Xmit success. If the Tx Interrupt enable bit is set, an interrupt is also asserted.*

Bit 7: Buffer Window Interrupt. *When set, this bit indicates that data has been read from the local buffer*

into the DMA FIFO and is ready to be read via the Bus Interface. If the associated interrupt enable bit has been set, an interrupt is asserted.

Bit 8: Not Used.

Bit 9: Rx On. *When set, this bit indicates that the Receiver is enabled. This bit remains set during active reception of a packet and turns 'off' at the end of reception if bit 12 Rx off is set.*

Bit 10: Tx On. *When set, this bit indicates that the Transmitter is enabled.*

Bit 11: SQE Quality Test Failed. *Is set low if and only if there is an SQE Test failure. Whenever this bit is set, if the Tx Int Enable bit (bit 2 of the Command Register) is HIGH, the Tx Int bit (bit 6 of the Status Register) will also be set and an interrupt will be issued [Refer Bit 4 (SQET Test Enable) of Transmit Header Byte 3.]*

Bit 12: No Tx Fail Indication. *Is set low if and only if a packet failed to be transmitted. This bit is set high by a Software or Hardware Reset, or by writing a one to the Tx Int Ack Bit (bit 6 of the Command Register). Errors which will cause this bit to be set low are those which result in failure to complete transmission of a packet, i.e. 1) 16 [consecutive] collisions, and 2) Babble Error with Tx Babble Int Enable set HIGH> Whenever this bit is set low, if the Tx Int Enable bit is HIGH, the Tx Int Bit will be set and an interrupt will be issued.*

If the NoTxFail bit is set low due to a Babble error, the transmitter will be turned off. The transmitter will not be turned off in the event of 16 consecutive collisions unless the packet is the last packet in the chain, i.e. bit 6 of its command byte is 0.

Once set, low, No Tx Fail stays low until:
(1) Hardware Reset is asserted;
(2) Software Reset is asserted;
(3) The local processor writes a one to bit 6 of the Command Register, Tx Int Ack.

If the transmitter has been turned off and the NoTxFail bit and/or the SQE pass Fail Bit is LOW, the Transmitter cannot be turned back on until the local processor clears the error bit by writing '1' to the Tx Int Ack Bit. This is to assure that the possibly serious error condition is noticed.

If a Babble Error occurs with Tx Babble Int Enable set LOW, transmission will not terminate and the No Tx Fail Bit will not be set.

If 16 consecutive collisions occurs and the 16 Collision Int Enable Bit is set LOW, NoTxFail Bit will be set low, but no interrupt will be given, nor will the Tx Int Bit be set.

Bit 13: DMA FIFO Full. *When set, this bit indicates that the DMA FIFO is full.*

Bit 14: DMA FIFO Empty. *When set, this bit indicates that the DMA FIFO is empty.*

Bit 15: FIFO Direction. *When set, this bit indicates that the DMA FIFO is in the read direction; when cleared, it indicates that the DMA FIFO is in the write direction. After hardware or software reset, this bit is cleared.*

Configuration Register 1, A3-0=001X

Bits 0-3: Buffer Code. *These four bits are the Buffer Window Code bits, which determine the source of Buffer Window register reads and the destination of buffer window register writes. Buffer code bits 3-0 should be set to '1000' by pointing to local buffer memory before turning FIFO to read direction to perform reads.*

Buffer Code Selection Table

Buffer Code Bits Buffer Window Reg.. Contents

3	2	1	0	
0	0	0	0	Station Address Register #1
0	0	0	1	Station Address Register #2
0	0	1	0	FCS Error Counter
0	0	1	1	Dribble Error Counter
0	1	0	0	Oversized Frame Error Counter
0	1	0	1	Reserved
0	1	1	0	Address PROM
0	1	1	1	Transmit End Area
1	0	0	0	Local Buffer Memory
1	0	0	1	Short Frame Error Counter
1	0	1	0	Excessive Deferral /Late Collision Counter
1	0	1	1	Transmit Collision Counter
1	1	0	0	Configuration Register 3
1	1	0	1	Product ID Register
1	1	1	0	Test Enable Register
1	1	1	1	Multi-Cast Address Filter Table

Bits 14-15: *These two bits define the match modes for the Receiver logic.*

15	14	Matchmode Description
0	0	Specific addresses only
0	1	Specific + broadcast addresses
1	0	Above + multicast addresses
1	1	Al frames (promiscuous Mode)

Configuration Register 2, A3-0 = 010X

Bit 0: ByteSwap. *The normal order for packing packet bytes into a 16 bit word is low byte first, i.e., the first byte of a packet is contained in bits 0 through 7, the second byte in bits 8 through 15. Setting this bit to a 1 causes the high and low order bytes to be swapped for data reads and writes to the Buffer Window Register when the 80C04A is in 16 bit mode. Control registers are not affected. This bit has no effect when the 80C04A is in 8 bit mode. Changing this bit will not affect the sequence of receive data bytes in the local buffer memory since the swap occurs on the system (Bus Interface) side of the buffer memory. This bit is both read and write.*

Bit 1: Auto Update REA. *If this bit is set to a 1, the Receive End Area Register will be updated whenever the DMA pointer register crosses a packet buffer page while reading data from the Receive section of the packet buffer. In this way, as buffer memory space is released by reading from it, free buffer space is automatically allocated to the Receive logic.*

Notes on Auto Update Feature

When the REA (Receive End Area) register is being automatically updated as the DMA pointer crosses a page boundary, instead of loading the new value of the DMA pointers high byte, the old value (prior to incrementing) is loaded into the REA. This results in setting the REA to the previous page rather than the current page. As an example, when the DMA pointer wraps around from FFFF to the Transmit End Area + 100 (hex), the REA will be set to FF (which is, again, the Previous page).

Updating of the REA is inhibited whenever reads occur in the transmit area of the packet buffer even if the Auto Update feature is programmed on. Updating of the REA is also inhibited when the FIFO Direction is WRITE.

Bit 2: Receive While Transmitting Disable: *When set to 1, the Receive-While-Transmitting function is disabled. The disabling function acts by masking the carrier sense signal to the receiver if the Rx-Tx-Disable bit is set and if the 80C04A's transmit enable signal, TXEN, is high. To perform a loopback test, the RX-TX-Disabled bit must be cleared to enable reception of the looped-back packet.*

Bit 3: CRC Error Enable. *When set, the receiver will accept packets with CRC errors, place them in the local buffer and indicate that a packet is available via the Rx Interrupt Status bit.*

Bit 4: Dribble Error. *When set, the receiver will accept packets with a byte alignment error.*

Bit 5: Pass Long/Short Errors. *This bit covers both short packet and long packet error conditions. When this bit is set HIGH, packets with long or short packet errors will be passed and stored in the buffer, provided they do not have other unpassable errors. If a long or short packet is accepted and stored in the Buffer, the Rx Int Bit will be set and, if the Rx Int Enable bit is HIGH, an interrupt will be issued.*

A short packet is one that has fewer than 60 bytes including Destination Address, Source Address, Length Field and Data Field, not including Preamble or CRC Fields. When this error occurs, if the packet is stored in the Buffer, bit 3 of Receive Header Byte 4 will be set HIGH.

A long packet is one that has more than 1514 bytes including Destination Address, Source Address, Length Field and Data Field, not including Preamble or CRC Fields. When this error occurs, if the packet is stored in the Buffer, bit 0 of Receive Header Byte 4 will be set HIGH.

Bit 6: Not Used. *This bit should be written to "0" for future compatibility.*

Bit 7: PreamSelect. *When this bit is a 0, which is the state after reset, the 80C04A automatically transmits an IEEE 802.3 compatible 64 bit preamble; when set to 1, the user must supply the preamble as part of the packet data. the preamble must still follow the 802.3 form in order to be recognized by other 80C04A's, but may have arbitrary length. Note that a minimum of 16 preamble bits are required by the 8005 on reception.*

Bit 8: Not Used.

Bit 9: RecCrc. *If set to a 1, received packets will include the CRC . If set to a 0, which is the state after reset, the 4 byte CRC will be stripped when received.*

Bit 10: XmitNoCrc. *If set to a 1, the Transmitter will not append the 4 byte frame check sequence to each packet transmitted. This is useful in local loopback to perform diagnostic checks, since it allows the software*

to provide its own CRC as the last four bytes of a packet to check the Receiver CRC logic. It is initialized to 0 after hardware or software reset.

Bit 11: Loopback. *This bit controls the External Loopback pin. When set to a 1, the loopback output pin is at Vol; after reset or when cleared to a 0, the External Loopback output pin is at Voh.*

Bit 12: CTRLO. *This bit controls the Control Output pin. When set to a 1, the CTRLO pin is at Voh; when cleared to 0 or after reset, this pin is at Vol.*

Bits 13-14: Not used. *Reserved for future use.*

Bit 15: Reset. *Writing a 1 to this bit is the same as asserting the hardware reset input. Reset should be followed by a 4 µs wait before attempting another access. Reads as a 0.*

Note: *There are two types of reset, Hardware Reset and Software Reset. The 80C04A will reset when the RESET* Pin, pin 16 is held LOW for a minimum pulse width of 100 nanoseconds (Hardware Reset), or the Reset Bit, is written HIGH (Software Reset). Reset can take up to 4 microseconds maximum to complete from the high going edge of the RESET* pulse. During this time the local processor should not access the chip.*

After a Hardware or Software Reset has completed, the chip is ready for configuration and initialization. The Reset Bit, like the RESET Pin, has a one-shot action. Once set to 1, it Initiates the Software Reset sequence which cannot be interrupted (except by a Hardware Reset).

Receive End Area Register, A3-0 = 0110

Bits 0-7: ReaPtr. *The Receive End Area pointer contains the high order byte of the local buffer address at which the Receive logic must stop to prevent writing over previously received packets. If the Receive logic reaches this address it will stop; the Receiver will be turned off and an interrupt will be issued. The Receiver can be re-started by freeing up buffer space and turning the Receiver back 'ON' again. It is both read and write.*

Buffer Window Register, A3-0 = 100X

This register provides access to the area specified by the Buffer Code bits (bits 0-3) in Configuration Register #1. When the Buffer Code points to either the buffer memory (Buffer Code =1000_2), or the address PROM (Buffer Code = 0110_2), the address of the data transferred through this register is determined by the DMA pointer. All Buffer Code registers are byte wide except data.

Receive Pointer Register, A3-0 = 101X

The Receive pointer provides a 16 bit address that points to the next buffer memory location into which data or header information will be placed by the Receive logic. The low order 8 bits contain the least significant byte of the address. Prior to enabling the Receiver, this register should be set to point to the beginning of the Receive Area in the local buffer. This initial value should be remembered by system software since it will be the address of the first byte of the header block of the first packet received. While receiving, the Receive pointer will be incremented for each byte stored into the local buffer. When the Receive pointer increments past hex FFFF the most significant byte will be set equal to the value of the Transmit End Area + 1 and the least significant byte will be set to 00. Reading this register may be done at any time. It should be written only when the receiver is idle.

Transmit Pointer Register, A3-0 = 110X

The Transmit pointer points to the current location being accessed by the Transmit logic. Before starting the Transmitter, software loads this register with the address of the beginning of a transmit packet chain.

Indirectly Accessed Registers

Infrequently used registers, such as, those normally loaded only when initially configuring the 80C04A, are accessed indirectly by first loading the Buffer Code bits in Configuration Register #1 with a code that points to the desired register. Reads and writes occur through the Buffer Window register. All indirect registers (a total of 18) are 8 bits wide, thus only D0-D7 are used.

Configuration Register 3

This is an indirectly-addressed register with an assigned Indirect Address of "C" hexidecimal (1100)

Bit 0: Auto Padding. *Transmitter will automatically pad those packets less than minimum frame length.*

Bit 1: SA Hash Table Enable. *With the Receiver in Multicast address match mode, setting this bit to 1 causes the hash table to be used for filtering all destination addresses independent of whether the address is a multicast address.*

Bit 2: SQE Test Enable. *Enable the Signal Quality Test.*

Bit 3: Sleep Mode. *Set to the sleep mode to save power. The contents of all resetable registers will be reset. The first write when the chip is in sleep mode will have no real effect except to take the chip out of sleep mode.*

Bit 4: *Not Used.*

Bit 5: 2nd Station Address Register Enable. *Setting this bit to 1 enables Station Address Register #2 for comparison purposes by the receiver. Once set a packet with a destination address matching either S.A Register #1 or S.A Register #2 will accepted by the receiver.*

Bit 6: Group Address Enable. *When this bit is set HIGH, the last four bits of the Destination Address field are masked out from address comparison. Other aspects of the address filtering remain unchanged.*

Note: Station Address Group Reception
Let a "station address group" be defined as a set of 16 station addresses which are identical in all bits but the last 4. (Station address, or physical address, implies that the first bit is 0.) the Group Address Enable Bit Enables/Disables Address Register comparison for a group of 16 station addresses, rather than an individual address. When this bit is set HIGH, the last four bits of the Station Address Register (bits 4-7 of the 6th byte) are masked. When the bit is cleared, address comparison is over all bits of the Address Register.

Bit 7: NPP Byte Swap. *The Next Packet Pointer Byte Swap bit. This bit is set LOW by Hardware or Software Reset. When this bit is set LOW, the Next Packet Pointer of all transmit and receive packets is stored in the Packet Buffer high byte first. When this bit is set HIGH, the byte order is reversed for the Next Packet Pointer only. The byte order of all other bytes are not affected by this bit.*

Station Address Register #1
This register is compatible with the 80C04 Station Address register. This register consists of six 8-bit registers which must be loaded through the Buffer Window Register. It is used by the receiver for address matching against the 6 byte destination address of a packet.

To load this Station Address register, first turn the Receiver off. To select this register, write the Buffer Code bits to 0. Next do 6 sequential byte writes to the Buffer Window register as follows: Write the most significant byte of the 6 byte Station Address: its low order bit, bit 0, will be the first bit received. Next write the remaining 5 bytes in descending order. To read this Station Address register, first turn the receiver off by setting 'bit 12' Rx off on the Command register and verifying that the Receiver is off. Then select this register by writing 0 to all the Buffer Code bits in Configuration Register #1. Do 6 sequential reads to the Buffer Window Register; the first byte read will be the most significant byte.

Station Address Register #2
This 2nd Station Address register is not available in the 80C04. Loading and reading of the 6 bytes of this register is done similarly to Station Address Register #1 except that the Buffer Code bits need to be written to "0001" binary. Normally, address comparisons will only be made against Station Address Register #1 by the Receiver. To activate this register for address comparisons bit 5 of Configuration Register #3 has to be written to a 1. Once activated, if the Receiver is not in promiscuous mode, destination addresses will be compared against both this register and Station Address Register #1. If a match occurs against either register, the packet will be received.

FCS Error Counter [1]
This is an 16 bit readable counter that counts the number of receive packets with FCS errors experienced by the Receiver. To read this counter, set the buffer code = 0010 and do a read to the buffer window register. For this counter, bit 0 is the least-significant bit of an sixteen-bit binary value and bit 15 is the most-significant bit. This counter stops counting upon reaching its maximum count value of 65535 and is reset to 0 when the counter is read.

Dribble Error Counter [1]
This is an 16 bit readable counter that counts the number of receive packets that have both alignment and FCS errors. A packet must have both errors for the Receiver to increment this counter. To read this counter, set the buffer code = 0011 and do a read to the buffer window register. For this counter, bit 0 is the least-significant bit of an sixteen-bit binary value and bit 15 is the most-significant bit. This counter stops counting upon reaching its maximum count value of 65535 and is reset to 0 when the counter is read.

Oversized Receive Frame Counter
This is an 8 bit readable counter that counts the number of receive packets with greater than 1514 bytes of data. To read this counter, set the buffer code = 0100 and do a read to the buffer window register. For this counter, bit 0 is the least-significant bit of an eight-bit binary value and bit 7 is the most-significant bit. This counter stops counting upon reaching its maximum count value of 255 and is reset to 0 when the counter is read.

Short Receive Frame Counter [1]
This is an 16 bit readable counter that counts the number of receive packets with less than 64 bytes of data including CRC. To read this counter, set the buffer code = 1001 and do a read to the buffer window register. For this counter, bit 0 is the least-significant bit of an sixteen-bit binary value and bit 15 is the most-significant bit. This counter stops counting upon reaching its maximum count value of 65535 and is reset to 0 when the counter is read.

Note: Both bytes of all 16-bit management counters are readable with BUSSIZE = 1 only. In 8-bit mode only the LSB of the counter can be read.

Excessive Defer/Late Collision Counter

Reading this register provides the count values of two 4 bit counters. One counter counts the number transmit packets that experience an excessive deferral condition. Excessive deferral is defined as deferring for a time greater than 3036 byte times in duration, (2428.8 micro seconds). The other counter counts late collisions. A late collision is a collision that occurs greater that 64 byte times, (51.2 micro seconds), into a transmission. Reading of both these counters is done simultaneously by setting the buffer code = 1010 and doing a read to the buffer window register. The excessive deferral count value appears as bits 3 through 0 with bit 0 being the LSB and bit 3 being the MSB. Bits 7 through 4 contain the late collision count value with bit 4 being the LSB and bit 7 being the MSB. Both counters stop counting upon reaching their maximum count value of 15 and are both reset at the same time whenever this register is read.

Transmit End Area Pointer

The 8-bit value of this pointer defines, with 256 location granularity, the end of the Transmit Packet Buffer area by specifying the highest value permitted in the most significant byte of the Transmit Pointer Register and, when loading a packet to be transmitted, the DMA Address register. It also indirectly defines the Receive Start Area address, since the Buffer Controller automatically calculates the high order byte of the address by adding 1 to the Transmit End Area pointer. To read or write this value, set Buffer Code = 0111, and do a read or write to the Buffer Window Register.

Product I.D. Register

The 8 bits of this register (read only) give the product and revision identification for this chip. For the 80C04A, bits 7-4 have the value of A hex and identify the product. Bits 3-0 will have the value of E hex and can change to reflect different revision levels. To read this register, set the buffer code = 1101 and do a read to the buffer window register.

Transmit Collision Counter

This is an 8 bit readable, writable counter that counts the number of collisions experienced by the transmitter. To read or write this counter, set the buffer code = 1011 and do a read or write to the buffer window.

Notes on Collision Counter

For this counter, bit 0 is the least-significant bit of an eight-bit binary value and bit 7 is the most-significant bit. Bit 7 is used as a Carry-link bit. To begin a collision sample period, the local processor clears the Collision Counter by writing 00 hex to it. The processor can read the value any time. The Counter generates an interrupt when bit 7 toggles to 1, provided that Tx Int Enable is HIGH. To run a multiple-read tally, the processor will read the Counter after an interrupt and test bit 7. If bit 7 is 1, 128 (decimal) is added to the tally. Reading the Counter clears bit 7 automatically after the read. The Tx interrupt is cleared by writing the Tx Int Ack bit HIGH. The preceding steps can be repeated to monitor long periods of time. To get the final result, read and add the entire Counter value to the tally. The Counter will lock up and cease to count if it reaches 255 decimal. Hardware and software Resets set the Counter to 255 decimal (disabled).

Multi-Cast Filter Table

The Multi-Cast Filter Table is 8 bytes of readable, writable register used by the receiver to evaluate multicast addresses. To read or write to this register, set the buffer code = 1111 and then do 8 consecutive reads or writes to the buffer window register. A description of how the Multi-Cast Filter Table is used is given on page 20 of the datasheet. The Multi-Cast Filter Table can be enabled for evaluation of non-multicast addresses by writing bit 1 of Configuration Register #3 to a 1.

Other Buffer Window Register Uses

Address PROM Access

The 80C04A supports access to up to 256 bytes of configuration data contained in a PROM or EEPROM. This can be used for any purpose, such as storing station addresses, register configurations, network connection data, etc. The address to the PROM is supplied by the DMA register through data bus bits D8-D15; the data lines from the PROM are connected to D0-D7. Chip select for the PROM is provided by output APEN. Before accessing this PROM, insure that Transmit, Receive and DMA sections of the 80C04A are disabled. Next load the PROM starting address which you wish to access into both the low byte and the high byte of DMA register. Set the Buffer Code bits in Configuration Register #1 to point to the address PROM. Each access to the Buffer Window register will chip enable the PROM, permitting reads. Successive accesses will increment the DMA register to point to the next byte in the PROM. If a 16 bit wide bus is used, the address supplied to the PROM will also be read on D8-D15.*

Buffer Memory Access

The normal state of the Buffer Code bits, once the 80C04A has been initialized with station addresses and buffer areas have been allocated, is with Buffer Memory selected. Access to the local buffer memory is provided by

Example of Chained Receive Frames

Bit #	7	6	5	4	3	2	1	0	
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	Upper byte of next packet pointer								
Addr. ptr 2	Lower byte of next packet pointer								
Header status	0	1	1	X	X	X	X	X	
Packet status	1	0	0	1	0	0	0	0	
Data									
"									
Addr. ptr 1	0	0	0	0	0	0	0	0	Next receive packet header goes here.
Addr. ptr2	0	0	0	0	0	0	0	0	
Header status	0	0	0	0	0	0	0	0	Last header in chain.
Packet status	0	0	0	0	0	0	0	0	

Packet Header Bytes

Transmit Header Command Byte

(Byte #3)

7	6	5	4	3	2	1	0
1	Chain Con-tinue	Data Fol-lows	SQET Tst Enable	Xmit Success Enable	16 Coll. Enable	Coll. Int. Enable	Babble Int. Enable

Receive Header Status Byte

(Byte #3)

7	6	5	4	3	2	1	0
0	Chain Con-tinue	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

Transmit Packet Status Byte

(Byte #4)

7	6	5	4	3	2	1	0
Done	Tx Single Coll	Tx Multiple Coll's	Tx OK But Deferred	CSN Dropout	16 Coll.	Colli-sion	Bab-ble

Receive Packet Status Byte

(Byte #4)

7	6	5	4	3	2	1	0
Done	Not Used	Not Used	Not Used	Short Frame	Drib. Error	CRC Error	Over-size

80C04A Configuration and Pointer Registers

Command (write only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Write	FIFO Read	Set Tx Off	Set Rx Off	Set Tst Int.	Set Tx On	Set Rx On	Set Tst Int	Buffer Window Ack	Tx Int Ack	Rx Int Ack	Tst Int Ack	Buffer Window Enable	Tx Int Enable	Rx Int Enable	Tst Int Enable

Status (read only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Dir	FIFO Empty	FIFO Full	No Tx Fail	SQET Fail	Tx On	Rx On	Set Tst Int	Buffer Window Int	Tx Int	Rx Int	Tst Int	Buffer Window Enable	Tx Int Enable	Rx Int Enable	Tst Int Enable

Configuration Register #1 (A3-0 = 001X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addr Match Mode	Addr Match Mode	*Not Used*										Buffer Code 3	Buffer Code 2	Buffer Code 1	Buffer Code 0

Configuration Register #2 (A3-0 = 010X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	Not Used	Not Used	Control Output	Loop-Back	Xmit No CRC	Recv. CRC	Not Used	Xmit No Pream	Not Used	Short Frame Enable	Drib. Error Enable	CRC Error Enable	Rx-Tx Disable	Auto Update WPP	Byte Swap

Configuration Register #3 (BCODE = 1100)

7	6	5	4	3	2	1	0
NPP Byte	Group Addr	S.A. Reg.#2 Enable	Not Used	Sleep	SQE Enable	S.A. Hash Enable	Auto Pad

Receive End Area Register (A3-0 = 0110 [2])

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	Receive End Area Pointer							

Receive Pointer Register (A3-0 = 101X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT RECEIVE BYTE															

Transmit Pointer Register (A3-0 = 110X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT TRANSMIT BYTE															

DMA Address Register (A3-0 = 111X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR SYTSEM READS OR WRITES															

Buffer Window Register (A3-0 = 100X [2])

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFFER CODE BITS DETERMINE SOURCE/DESTINATION FOR READS AND WRITES															

NOTES: 1. In 16 bit mode address A0 is a don't care for all registers except REA.
2. Both 8 and 16 bit modes.

the DMA register, which automatically increments after each byte or word transfer. For reads and writes to the buffer memory, the following setup procedures are recommended:

Setup for Local Processor Buffer Write, [2]

Set FIFO Direction to Write (if different) [1]
Set Indirect Address to 8 (if different) [1]
Set DMA pointer
Perform data writes to buffer window register,

Setup for Local Processor Buffer Reads,

Table 3 — 80C04 MOTOROLA MODE BUS INTERFACE (BUSMODE = 0)

BUSSIZE	*CS**	*UDS**	*DS* or LDS**	*A0*	*D15-D8*	*D7-D0*
X[1]	*1*	*X*	*X*	*X*	*–[2]*	*–[2]*
1	*0*	*1*	*1*	*X*	*–[2]*	*–[2]*
0	*0*	*X*	*1*	*X*	*–[2]*	*–[2]*
0	*0*	*X*	*0*	*0*	*—*	*LO BYTE*
0	*0*	*X*	*0*	*1*	*—*	*HI BYTE*
1	*0*	*0*	*0*	*X*	*HI BYTE*	*LO BYTE*
1	*0*	*1*	*0*	*X*	*—*	*LO BYTE*
1	*0*	*0*	*1*	*X*	*HI BYTE*	*—*

NOTES:

1. *X = Don't Care.*
2. *CS* and either UDS* or LDS*/DS* (or both) must be affirmed (low) to begin a read or write operation.*

Station Address Register Format

7	6	5	4	3	2	1	0
MOST SIGNIFICANT BYTE STATION ADDRESS REGISTER 0 BYTE 0 BUFFER CODE = 0000							
STATION ADDRESS REGISTER 0 BYTE 1 BUFFER CODE = 0000							
STATION ADDRESS REGISTER 0 BYTE 2 BUFFER CODE = 0000							
STATION ADDRESS REGISTER 0 BYTE 3 BUFFER CODE = 0000							
STATION ADDRESS REGISTER 0 BYTE 4 BUFFER CODE = 0000							
STATION ADDRESS REGISTER 0 BYTE 5 BUFFER CODE = 0000 LEAST SIGNIFICANT BYTE							

Set FIFO Direction to Write (if different)[1]
Set Indirect Address to 8 (if different)[1]
Set DMA pointer
Set FIFO Direction to Read
Perform data reads to buffer window register

Notes: [1] Adjacent steps marked with [1] can be permuted. Order shown is recommended.

[2] To avoid improper termination of Buffer Write operations: if Direction Bit = zero (write mode), FIFO Empty Bit must be one (empty).

ASYNCHRONOUS BUS CONTROL

The 80C04A supports asynchronous bus control via the READY/DTACK pin. By using READY/DTACK*, the cycle time minimums listed in the tables A thru' J need not be observed. READY/DTACK* takes care of these cycle times. This greatly simplifies the task of interfacing to the 80C04A and also results in a higher overall data rate. To achieve the highest possible data rate, all data transfers should terminate within 100 ns of READY/DTACK* being asserted. This permits a sustained system bus transfer rate of 8 Mbytes/sec in 16 bit mode.*

POWER CONSERVATION

Since the 80C04A may be used where the power load is an important design consideration, such as battery-operated equipment (lap-tops) or heat-sensitive applications, power considerations are of primary importance.

The CMOS Technology provides power saving over NMOS Technology. Additional power can be conserved by setting the SLEEP bit in the Configuration Register 3.

Operating Power Load

The maximum operating load is 300 mW. This is under maximum load conditions where the 80C04A is in Loopback Mode with Rx-Tx enabled (transmitting and receiving back-to-back minimum-length packets), and transferring all received packets to the local processor.

Sleep (Power Down) Mode

The Power Down State can be forced into by setting the SLEEP bit in Configuration register 3 to a 1. Except for the Multi-cast Filter and the Station Address Registers, all register and pointer settings will be reset. The first write to any register when in Power Down mode will NOT have any other effect besides making the chip come up in its idle state and resetting the SLEEP bit back to 0.

Full Featured Mode

Pin 47 is the Full Feature pin. When this pin is set high or left disconnected the following functions are disabled:

a. IOR (LDS*) input is ignored if BUSMODE = 0 (pin 50)*

b. BHE (UDS*) input is ignored (pin 53)*

When set low, the new bus interface features of the 80C04A are enabled.

With the 80C04A in full feature mode (FFEA pin 47 set low), an improved Bus Interface provides byte-wide data writes in 16-bit mode. Improved Intel compatibility is provided via the Byte High Enable (BHE*) pin allowing byte wide writes in 16-bit mode. Improved Motorola compatibility also provides for byte-wide writes in 16-bit mode and therefore requires no additional circuitry to interface to Motorola's 68xx (also 6502) and 680xx buses. For Motorola mode the LDS* (Lower Data Strobe) function is added to the original IOR* functionality of pin 50 in the 8005. Both the UDS* (Upper Data Strobe) function for Motorola compatibility and the BHE* function for Intel compatibility are combined using pin 53 of the 80C04A.*

TABLE 1 — 8005/80C04A BUS INTERFACE CONTROL PIN DIFFERENCES

8005 Pin#	Intel Function 80C04A	Intel Function 8005	Motorola Function 80C04A	Motorola Function 8005
50	IOR*	IOR*	LDS*	—
53	BHE*	NC	UDS*	NC
54	NC	IACK*	NC	IACK*
48	NC	Termct	NC	Termct*

NC — No Connect.

Data is written from the system bus to the system bus to the 16-bit registers depending on the state of the bus control signals. Tables 2 & 4 show the states of the BUSSIZE, CS, BHE*, and AO pins, which bytes of the registers are written under the given states, and whether the data for the register write comes from the D0-07 or the D8-D15 pins. This table is valid for all register writes except for data writes to the packet buffer. To perform a byte write 16-bit mode to the packet buffer, the data must occur on data pins D0-D7 and the BHE*/UDS* pin 53 must be driven high. Pins 50 (IOR*/LDS*) and 55 (A0) are ignored for byte writes to the packet buffer.*

For both FIFO and register reads in 16-bit mode, the BHE/ UDS* pin 53 is ignored and 2 bytes of data or both the high and low bytes of a 16-bit register are read.*

BUSMODE configures the 80C04A for Intel (BUSMODE = 1) or Motorola (BUSMODE = 0) compatible control signals. In Figure 1, pins with dual functions have dual names. The first name is for BUSMODE = 1 (Intel); the names in parenthesis apply to BUSMODE = 0, Motorola.

TABLE 2 — 80C04A INTEL MODE BUS INTERFACE (BUSMODE = 1)

Bussize	CS*	BHE*	A0	D15 -D8	D7-D0
X[1]	1	X	X	–[2]	–[2]
0	0	X	0	—	LO BYTE
0	0	X	1	—	HI BYTE
1	0	0	0	HI BYTE	LO BYTE
1	0	1	0	—	LO BYTE
1	0	0	1	HI BYTE	—
1	0	1	1	—	—

Notes:

1. X = Don't Care.
2. CS* and either IOR* or IOW* must be asserted (low) to begin a read or write operation.

Multi-Cast Filter Algorithm

Hashing Function and 64 bits of Multi-Cast Filter Register are used for multicast address filtering. The filtering method is applied only to multicast addresses, or if so programmed to Station ID's. The first bit of the address will be a 1 for multicast addresses, 0 for Station ID's.

The Hashing Function works, by using the CRC Checker. The CRC value from the CRC Register is taken after only the Destination Address has been entered into the CRC calculation. Using Bits 2-7 inclusive of this CRC value, (where bit 0 is the data entry end of the register and bit 31 is the result exit end), these bits are used to address the Hash Table Register. Bits 7 thru 5 select which byte of the Hash Table is being addressed and bits 4 thru 2 select which bit of that byte is being addressed. CRC bit 7 represents the MSB of the byte address and CRC bit 4 represents the MSB of the bit address. If the stored value selected is a 1, the packet will be accepted; if a 0, rejected. The local processor sets data into the Hash Table Register to select the multicast addresses, or if so programmed the station ID's, that will pass.

The Hash Table Register is an indirectly-addressed shift register accessed through the Buffer Window with Indirect Address IA3-IA0 = 1111, F hex. This is a write-read register. Data is loaded into this register in 8 sequential transfers of one byte each over data lines D0-D7. The bytes are loaded least-significant byte first with D0 being the least-significant bit of each byte.

Absolute Maximum Stress Ratings

Temperature:
Storage ..... –65°C to +150°C
Under Bias ..... –10°C to +80°C
All Inputs and Outputs with
Respect to V_{SS} ..... +6 V to –0.3 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Operating Charateristics (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Condition
I_{IL}	Input/Output Leakage		10 200	µA µA	$V_{IN} = V_{CC}$ $V_{IN} = 0.1$ V
I_{CC}	Active I_{CC} Current @ $T_A = 0°C$		40	mA	CS* = V_{IL}, Outputs Open $T_A = 0°C$
	Standby I_{CC} Current @ $T_A = 0°C$		TBD		
V_{IL}	Input Low Voltage	–0.3	0.8	V	
V_{IH1}	Input High Voltage (except TXC*, RXC, CLK)	2.0	V_{CC} + 1	V	
V_{IH2}	Input High Voltage (TXC*, RXC, CLK)	3.5	V_{CC} + 1	V	
V_{OL1}	Output Low Voltage (except D_{0-15} and READY)		0.40	V	$I_{OL} = 4.0$ mA
V_{OH1}	Output High Voltage (except D_{0-15} and READY)	2.4		V	$I_{OH} = 4.0$ mA
V_{OL2}	Output Low Voltage (D_{0-15})		0.40	V	$I_{OL} = 2.0$ mA
V_{OH2}	Output High Voltage (D_{0-15})	2.4		V	$I_{OH} = 2.0$ mA
V_{OL3}	Output Low Voltage (READY)		0.40	V	$I_{OL} = 16$ mA
V_{OH3}	Output High Voltage (READY)	2.4		V	$I_{OH} = 16$ mA

A.C. Test Conditions

Output Load:
AD0-AD7, I(load) = ± 200 µA
C(load) = 50 pF.
All Other Outputs: 1 TTL Gate and C(load) = 100 pF.
Input Rise and Fall Times (except TXC, RXC, CLK):
10 ns maximum.
Input Rise and Fall Times (TXC, RXC, CLK):
5 ns maximum.
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V

Recommended Operating Conditions

V_{CC} Supply Voltage	5V ± 5%
Ambient Temperature	0°C to 70°C

Capacitance [1] Ambient Temperature = 25°C, F = 1 MHz

Symbol	Parameter	Limits		Unit	Test Condtion
		Min.	Max.		
C_{IN}	Input Capacitance		15	pF	V_{IN} = 0
C_{OUT}	Output Capacitance		15	pF	V_{OUT} = 0

Electrostatic Discharge Characteristics

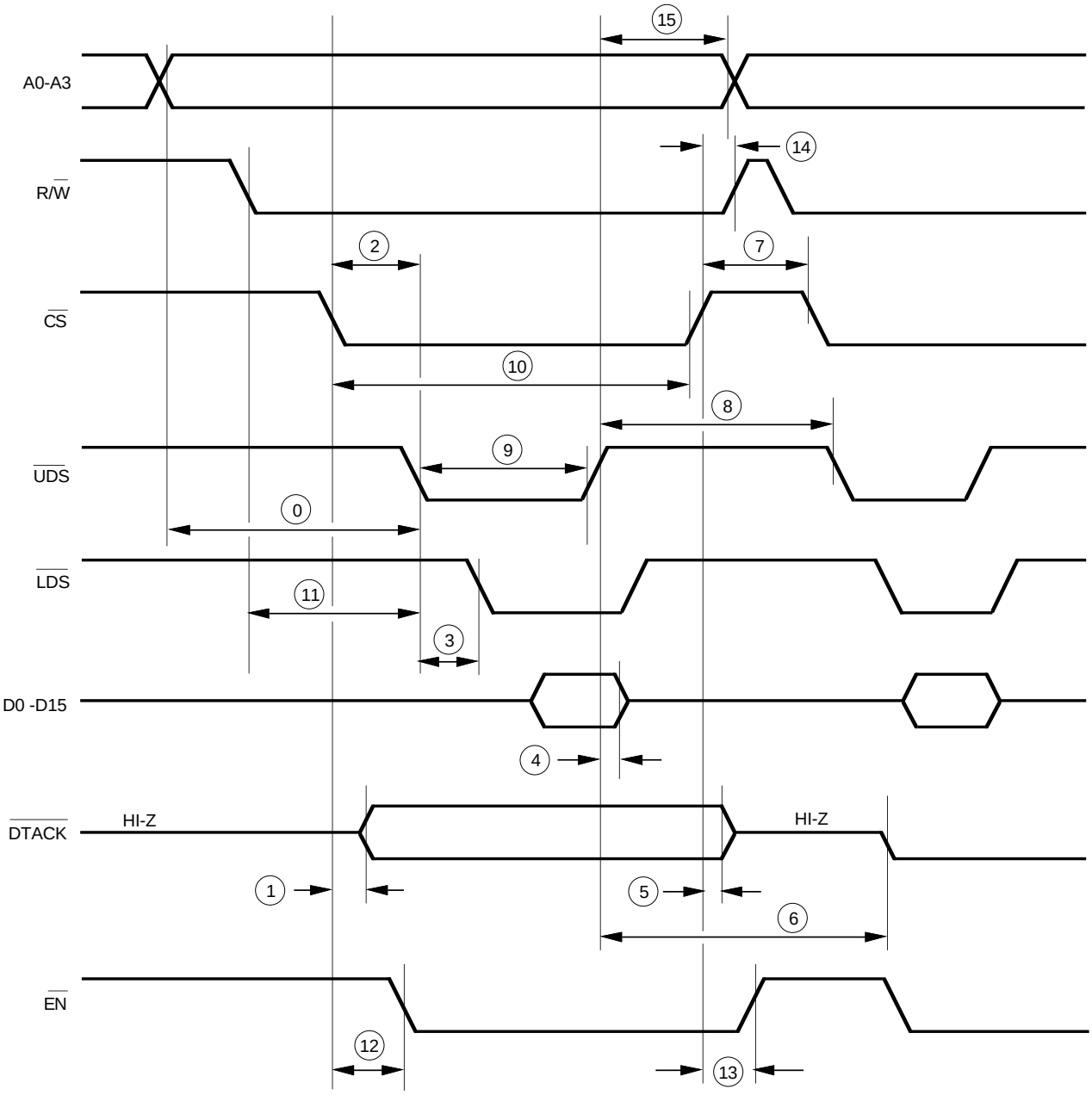
Symbol	Parameter	Value	Test Condtion
V_{ZAP} [2]	E.S.D. Tolerance	> 2000 V	Mil-STD 883 Meth. 3015

NOTES: 1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

Motorola Mode Full Feature — Write Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
0	TAVCSL	Address Setup	0		ns
1	TCSLDTV	$\overline{CS}$ to DTACK Valid		25	ns
2	TCSLDSL	$\overline{CS}$ Setup to $\overline{UDS}$/$\overline{LDS}$	0		ns
3	DSSKEW	$\overline{UDS}$ to $\overline{LDS}$ ($\overline{LDS}$ to $\overline{UDS}$) Skew		25	ns
4	TDSHDX	Data Hold Time	15		ns
5	TCSHDTZ	$\overline{DTACK}$ HI-Z Delay		10	ns
6	TDSHDTL	Write Recovery Time a. FIFO Data Write b. Configuration Regs c. Pointer Regs		 475 475 675	 ns ns ns
7	TCSHCSL	$\overline{CS}$ High Time [1]	0		ns
8	TDSHDSL	$\overline{UDS}$/$\overline{LDS}$ High Time	100		ns
9	TDSLDSH	$\overline{UDS}$/$\overline{LDS}$ Low Time	100		ns
10	TCSLCSH	$\overline{CS}$ Pulse Width	100		ns
11	TRWLDSL	R/$\overline{W}$ Setup Time	5		ns
12	TCSLENL	$\overline{EN}$ Assert Delay		20	ns
13	TCSHENH	$\overline{EN}$ Deassert Delay		25	ns
14	TCSHRWH	R/W* Hold Time	0		ns
15	TDSHAX	Address Hold Time	0		ns

NOTES:
1. $\overline{CS}$ can remain low while the R/W, $\overline{UDS}$, and $\overline{LDS}$ pins are used to signal the start and finish of an I/O operation. DTACK will remain valid as long as $\overline{CS}$ is low.



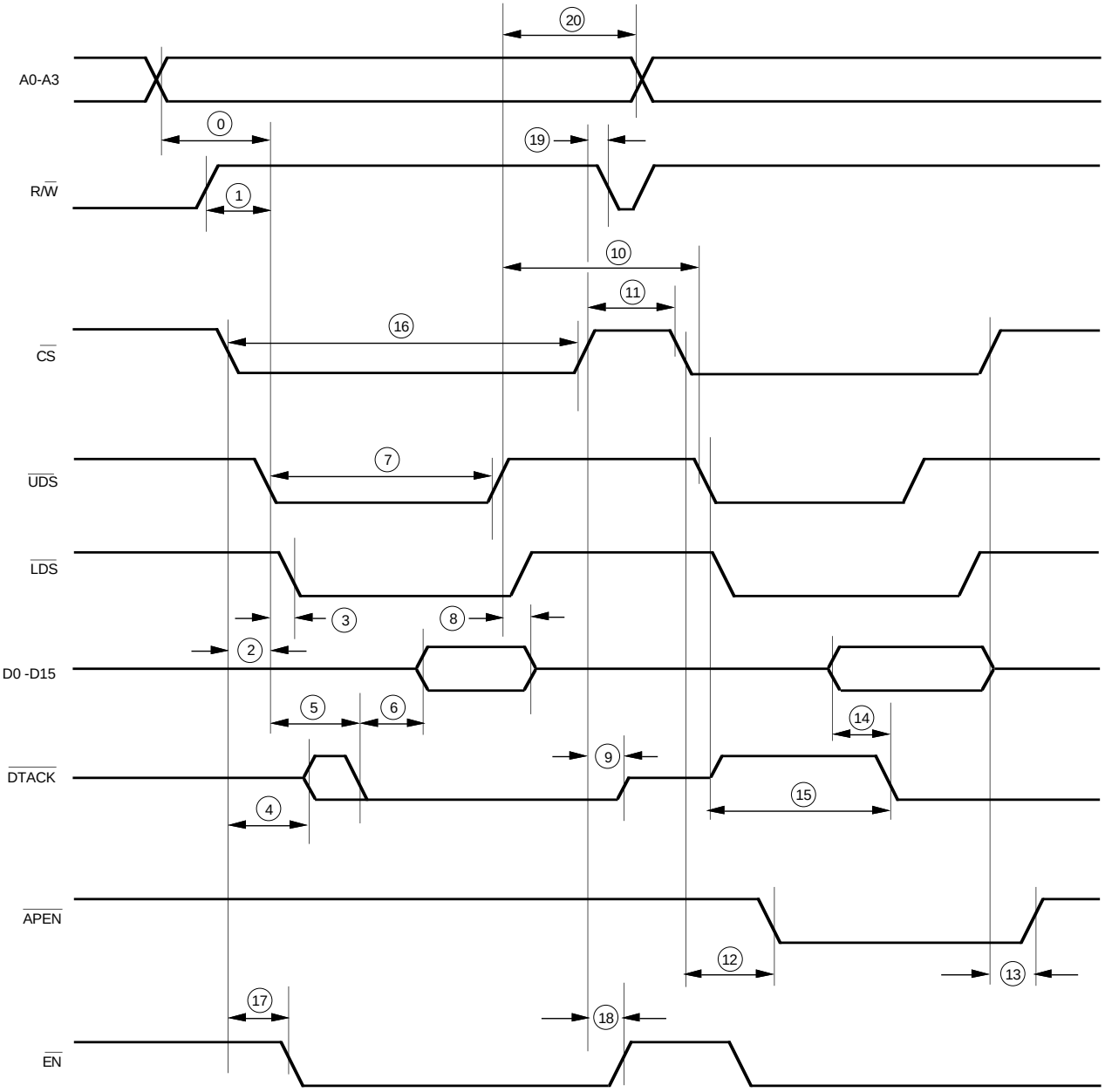
Moto Mode — 16 bit — Full Featured — Write Cycle

Motorola Mode Full Feature — Read Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
0	TAVCSL	Address Setup Time	0		ns
1	TRWHDSL	R/$\overline{W}$ Setup Time	5		ns
2	TCSLDSL	$\overline{CS}$ Setup to $\overline{UDS}$/$\overline{LDS}$	0		ns
3	DSSKEW	$\overline{UDS}$ to $\overline{LDS}$ ($\overline{LDS}$ to $\overline{UDS}$) Skew[2]		25	ns
4	TCSLDTV	$\overline{CS}$ to $\overline{DTACK}$ Valid		25	ns
5	TDSLDTV	$\overline{DTACK}$ Assert Delay a. FIFO Read[3] b. Configuration Regs c. Pointer Regs	 25	 475 675	ns ns ns ns
6	TDTLDV	$\overline{DTACK}$ Assert to Data Valid		5	
7	TDSLDSH	$\overline{UDS}$/$\overline{LDS}$ Low Time[2]	100		ns
8	TDSHDX	Data Hold Time	5		ns
9	TCSHDTZ	$\overline{DTACK}$ Hi-Z Delay		10	ns
10	TDSHDSL	$\overline{UDS}$/$\overline{LDS}$ High Time[2]	100		ns
11	TCSHCSL	$\overline{CS}$ High Time[1]	0		ns
12	TCSLAPL	$\overline{APEN}$ Assert Delay		100	ns
13	TCSHAPH	$\overline{APEN}$ Deassert Delay		100	ns
14	PRAVDTL	PROM READ Address Valid before $\overline{DTACK}$ Assert	250	475	ns
15	PRRDDTL	PROM Read $\overline{DTACK}$ Assert Delay		1125	ns
16	TCSLCSH	$\overline{CS}$ Low Time	100		ns
17	TCSLENL	EN* Assert Delay		20	ns
18	TCSHENH	EN* Deassert Delay		25	ns
19	TCSHRWL	R/W* Hold Time	0		ns
20	TDSHAX	Address Hold Time	0		ns

NOTES:

1. $\overline{CS}$ can remain low while the R/$\overline{W}$, $\overline{UDS}$, and $\overline{LDS}$ pins are used to signal the start and finish of an I/O operation. DTACK will remain valid as long as $\overline{CS}$ is low.
2. In 8-bit mode only LDS is used. UDS is a “don’t care”.
3. Upon switching the FIFO to the read direction, the first data read will typically require approximately 475 ns. Prefetches are attempted for subsequent data reads and if the prefetch is completed before the next read occurs, $\overline{DTACK}$ will assert within 25 ns of $\overline{UDS}$/$\overline{LDS}$ going low.



Moto Mode — Full Feature — Read Cycle

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{CC} range, unless otherwise specified)

Table A. Moto Mode Non-Full Feature — Write Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVCSL	Address Setup Time	0		ns
2	TRWLCSL	R/W* Setup Time	5		ns
3	TCSLCSH	CS* Pulse Width	100		ns
4	TDVCSH	Data Setup Time	0		ns
5	TCSHDX	Data Hold Time	15		ns
6	TCSLDTL	DTACK* Assertion Delay[3]		25	ns
7	TDTHDTZ	DTACK* Hi-Z Delay		10	ns
8	TCSHAX	Address Hold Time	0		ns
9	TCSHRWX	R/W* Hold Time	0		ns
10	TCSHCSL	CS* High Time	100		ns
11	TCSHDTL	Write Recovery Time: a. FIFO Data Write b. Configuration Regs [1] c. Pointer Regs. [2]		 475 475 675	ns ns ns ns
12	TCSLENL	EN* Assert Delay		20	ns
13	TCSHENH	EN* Deassert Delay		25	ns
14	TCSLDTV	CS* Assert to DTACK* Valid		20	ns

NOTES:

1. Configuration Registers are: Command/Status Register, Configuration Register #1, #2, #3, Product IO Register, Station Address Registers, Hash Table Registers, Test Enable Register, and Transmit Collison Counter.
2. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA register. If BUSSIZE = 0, subtract 600 ns.
3. The trailing edge of CS* initiates an internal write sequence. Should another CS* occur during this time, the assertion of DTACK* will be delayed until the internal write sequence has finished (Ref. #12, TCSHDTL).

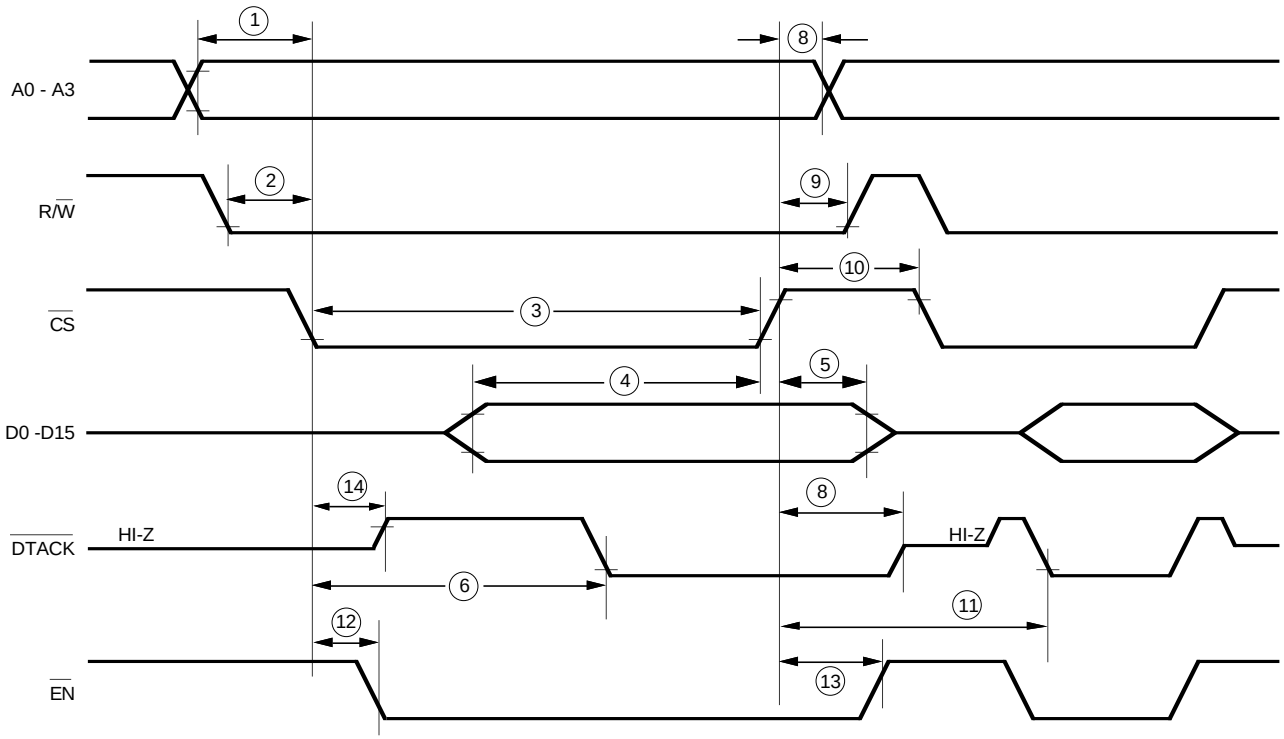


Figure A. Bus Write Cycle Timing Diagram — Busmode = 0, FFEA* = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{CC} range, unless otherwise specified)

Table B. Moto Mode Non-Full Feature — Read Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVCSL	Address Setup Time	0		ns
2	TRWHCSL	R/W* Setup Time	5		ns
3	TCSLDTL	DTACK* Assert Delay a. FIFO Data[1] b. Configuration Regs.[2] c. Other Pointer Regs.[3]		 25 475 675	ns ns ns ns
4	TDTLDV	Time from DTACK* Asserted to Data Valid		15	ns
5	TCSLCSH	CS* Pulse Width	100		ns
6	TDTHDTZ	DTACK* Hi-Z Delay		10	ns
7	TCSHDZ	Data Hi-Z Delay		100	ns
8	TCSHDX	Data Hold Time	5		ns
9	TCSHRWX	R/W* Hold Time	0		ns
10	TCSHAX	Address Hold Time	0		ns
11	TCSHCSL	CS* High Time	100		ns
12	TCSLAPL	APEN* Assert Delay		100	ns
13	TCSHAPH	APEN* Deassert Delay		100	ns
14	TCSLENL	EN* Assert Delay		20	ns
15	TCSHENH	EN* Deassert Delay		25	ns
16	TCSLDTV	CS* Assert to DTACK* Valid		20	ns
17	PRADRVD	PROM Address Valid to DTACK Assert	250	475	ns
18	PRRDRDY	PROM Read DTACK Assert Delay		1125	ns

NOTES:
1. The BIU prefetches one word (byte) of FIFO data. Thus, data is generally available immediately and DTACK* will assert within 50 ns. Following the read, the BIU will fetch the next word (byte) of data. Should another data read occur before the BIU has completed the prefetch, DTACK* will be delayed until the prefetch is completed. The assert delay in this case is 650 ns max (450 ns in 8 bit mode).
2. Configuration Registers are: Command/Status Register, Configuration Register #1 & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers.
3. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register.

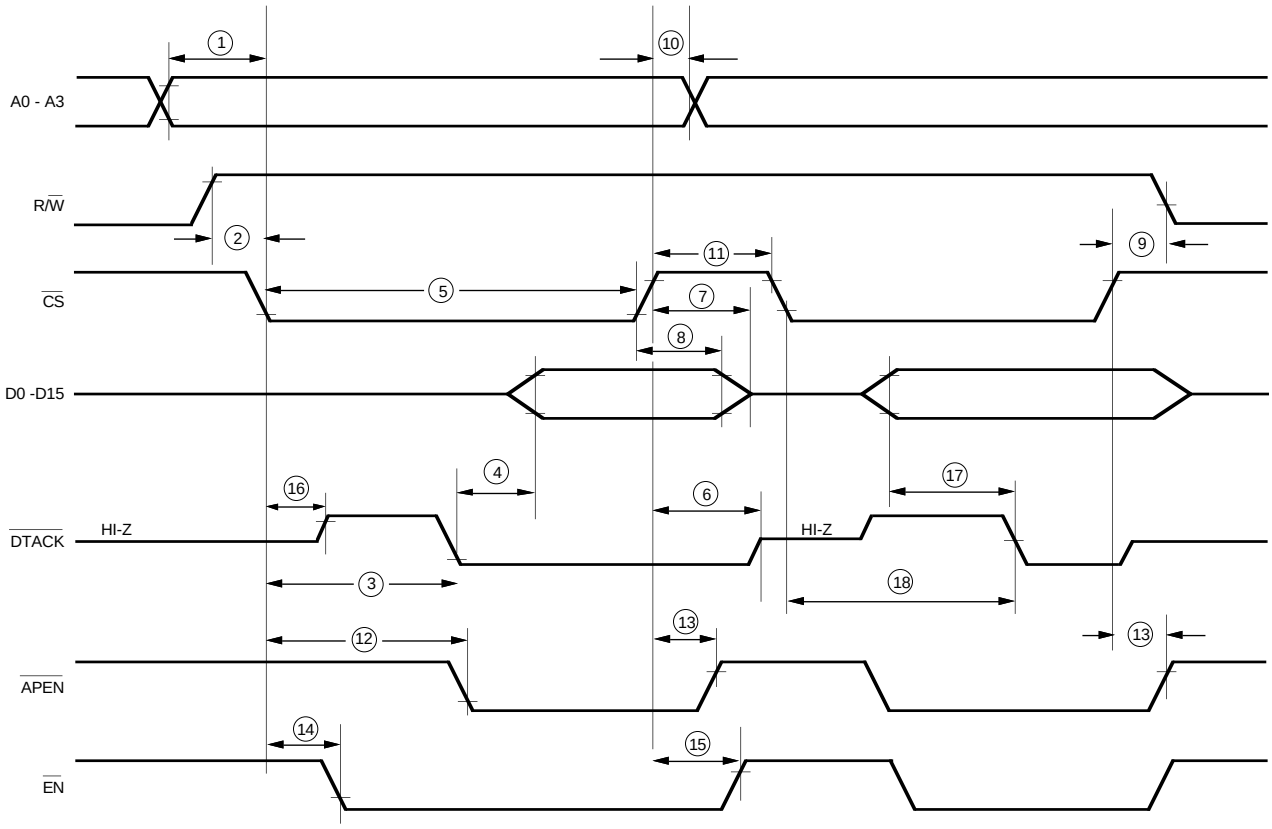


Figure B. Bus Read Cycle Timing Diagram — BUSMODE = 0, FFEA* = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{CC} range, unless otherwise specified)

Table C. Intel Mode — Write Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVWL	Address, BHE* Setup Time[5]	0		ns
2	TCSLWL	CS* Setup Time	5		ns
3	TWLWH	IOW* Pulse Width	100		ns
4	TDVWH	Data Setup Time	0		ns
5	TWHDX	Data Hold Time	15		ns
6	TCSLRYV	IOW* Asserted to READY Valid[3, 4]		25	ns
7	TCSHRYZ	READY Delay to Hi-Z		20	ns
8	TWHAX	Address, BHE* Hold Time[5]	0		ns
9	TWHCSH	CS* Hold Time	5		ns
10	TWHWL	IOW* High Time	100		
11	TWHRYH	Write Recovery Time: a. FIFO Data Write b. Configuration Regs. [1] c. Pointer Registers. [2]		 475 475 675	ns ns ns ns
12	TCSLENL	EN* Assert Delay		20	ns
13	TCSHENH	EN* Deassert Delay		25	ns

NOTES:

1. Configuration Registers are: Command/Status Register, Configuration Register #1, #2, #3, Station Address Registers, Hash Table Registers, Test Enable Register, Product ID Register, and Transmit Collison Counter.
2. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA Register. If BUSSIZE = 0, subtract 600 ns.
3. The trailing edge of IOW* initiates an internal write sequence. Should another IOW* occur during this sequence, READY de-asserts (Ref. # 6 TWLRYL) and then asserts after the internal write sequence has finished (Ref. #12 TWHRYH). If the subsequent IOW* does not occur until after the internal write sequence has ended, then Ref. # 6 TWLRYL has no meaning since READY does not de-assert under this condition.
4. With a loading of 15pf, the maximum TWLRYV is reduced to 15 ns.
5. The BHE* pin is functional only when the chip is in full feature mode as described on pages 16 and 19. Otherwise it is ignored.

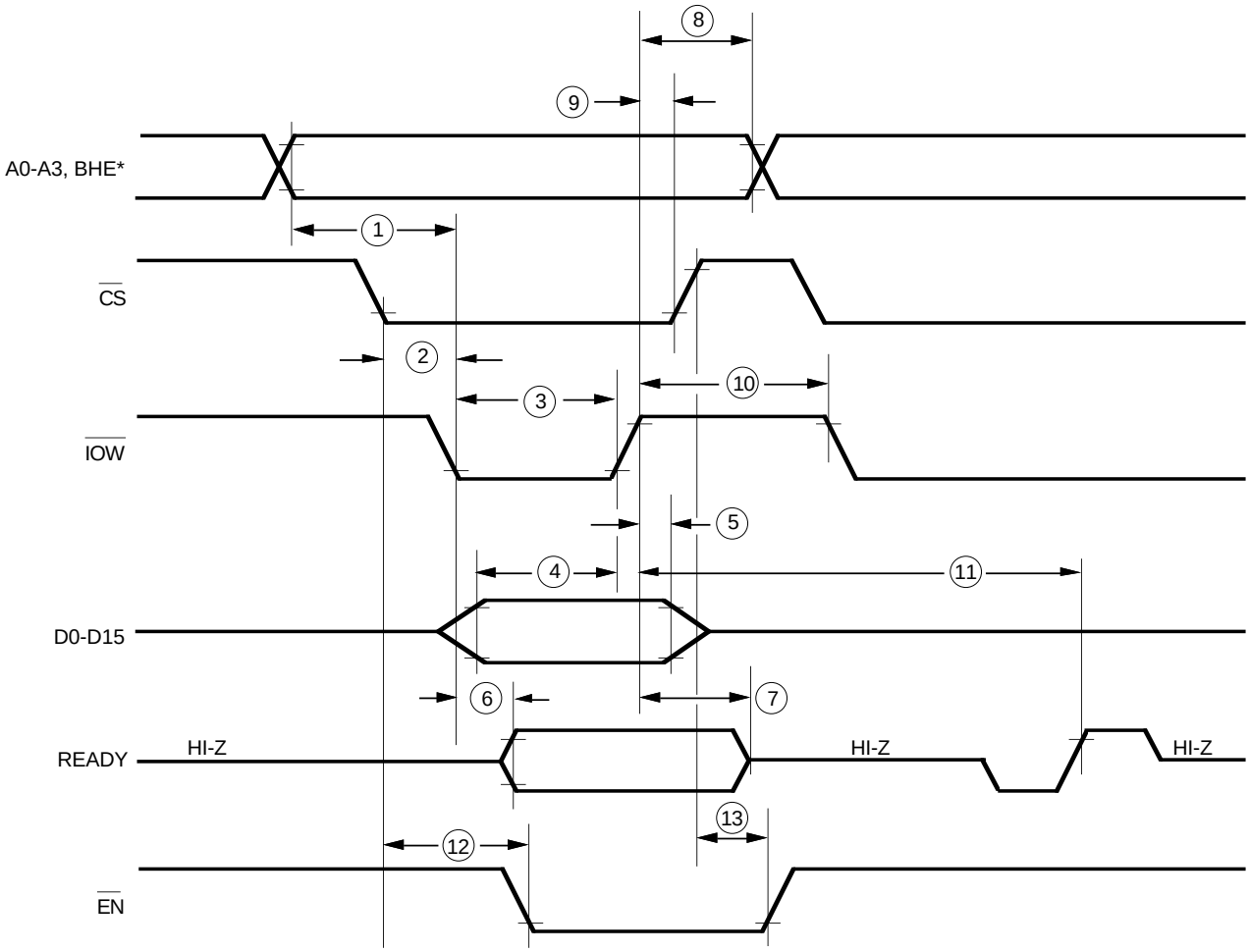


Figure C. Bus Write Cycle Timing Diagram — Busmode = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{CC} range, unless otherwise specified)

Table D. Intel Mode — Read Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVRL	Address Setup Time	0		ns
1a	TCSLRL	CS* Setup Time	5		ns
2	TRHRL	IOR* High Time	100		ns
3	TRLRYH	READY Assert Delay a. FIFO Data [1, 4] b. Configuration Regs.[2] c. Pointer Registers.[3]		 20 475 675	ns ns ns ns
4	TRLRYL	READY Deassertion Delay [4]		25	ns
5	TRYHDV	READY Assert to Data Valid		10	ns
6	TCSHRYZ	READY Delay to Hi-Z		15	ns
7	TRHDX	Data Hold Time	5		ns
8	TRHDZ	Data Delay to Hi-Z		15	ns
9	TRHAX	Address Hold Time	0		ns
10	TRHCSH	CS* Hold Time	0		ns
11	TRLRH	IOR* Pulse Width	100		ns
12	TRLAPL	APEN* Assert Delay		100	ns
13	TRHAPH	APEN* Deassert Delay		100	ns
14	TCSLENL	EN* Assert Delay		20	ns
15	TCSHENH	EN* Deassert Delay		25	ns
16	PRADRVR	PROM Address Valid to READY	250	475	ns
17	PRRDRY	PROM Read READY Assert Delay		1125	ns

NOTES:

1. The BIU prefetches one word (byte) of FIFO data. Thus, data is generally available immediately and READY will not de-assert during a data read. Following the read, the BIU will fetch the next word (byte) of data. Should another data read occur before the BIU has completed the prefetch, READY will first de-assert and then assert after the prefetch is completed. The assert delay in this case is dependent upon the amount of receive and or transmit activity of the 80C04A.
2. Configuration Registers are: Command/Status Register, Configuration Register #1, #2, #3, Hash Table Registers, Product ID Register, Station Address Registers, Test Enable Register, and Transmit Collision Counter.
3. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register, and DMA Register.
4. With a loading of 15pf, the maximum TRLRYL or TRLRYH is 15 ns.

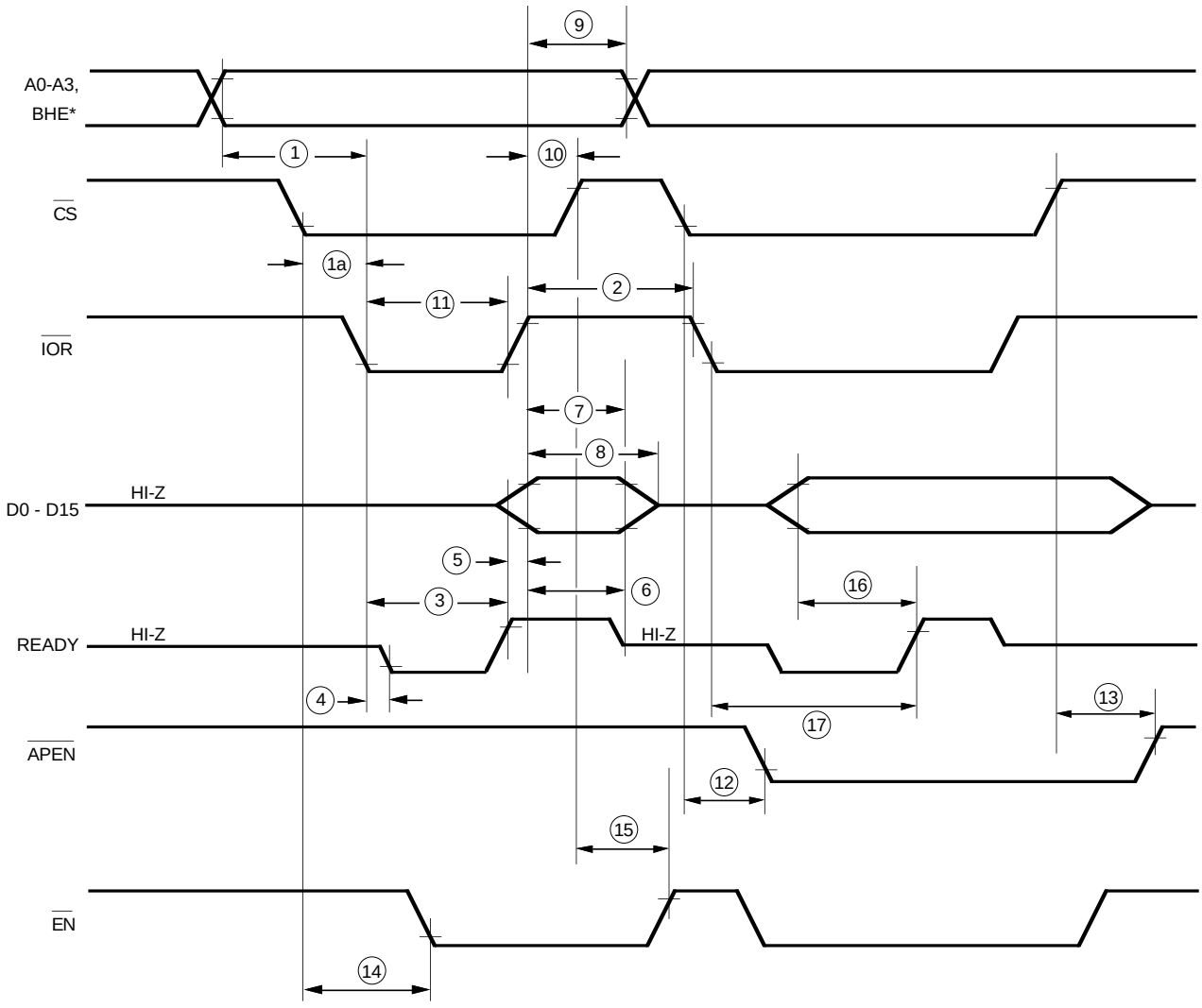


Figure D. Bus Read Cycle Timing Diagram — Busmode = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{CC} range, unless otherwise specified)

Table E. Local Buffer Read or Write Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRSLAX	Row Address Hold Time	75		ns
2	TAVRSL	Row Address Setup Time	100		ns
3	TRSHRSL	RAS* Pulse Width High	195		ns
4	TCSLAX	Column Address Hold Time	35		ns
5	TAVCSL	Column Address Setup Time	25		ns
6	TCSHCSL	CAS* Pulse Width — High	70		ns
7	TCSLCSH	CAS* Pulse Width — Low	125		ns
8	TAZGL	Address Hi-Z to G* Low Time	0		ns
9	TGLCSH	G* Setup Time to CAS*	75		ns
10	TGLDV	G* to Data Valid		40	ns
11	TCSHDX	Data Hold from CAS Deassert	0		ns
12	TCSHDZ	Data Hi-Z from CAS Deassert		35	ns
13	TAVAV	Read or Write Cycle Time a. Single Cycle b. Page Mode	 600 200		 ns ns
14	TDVWL	Data Setup Time	20		ns
15	TWLDX	Data Hold Time	70		ns
16	TWLWH	Write Pulse Width	75		ns
17	TCSLWL	CAS* Setup to W*	70		ns
18	TWLCSH	Write Setup Time	50		ns
19	TRSLRSL	RAS* Cycle Time	600		ns

NOTE: TMS 4464-10, –12 or equivalent satisfies the above timing.

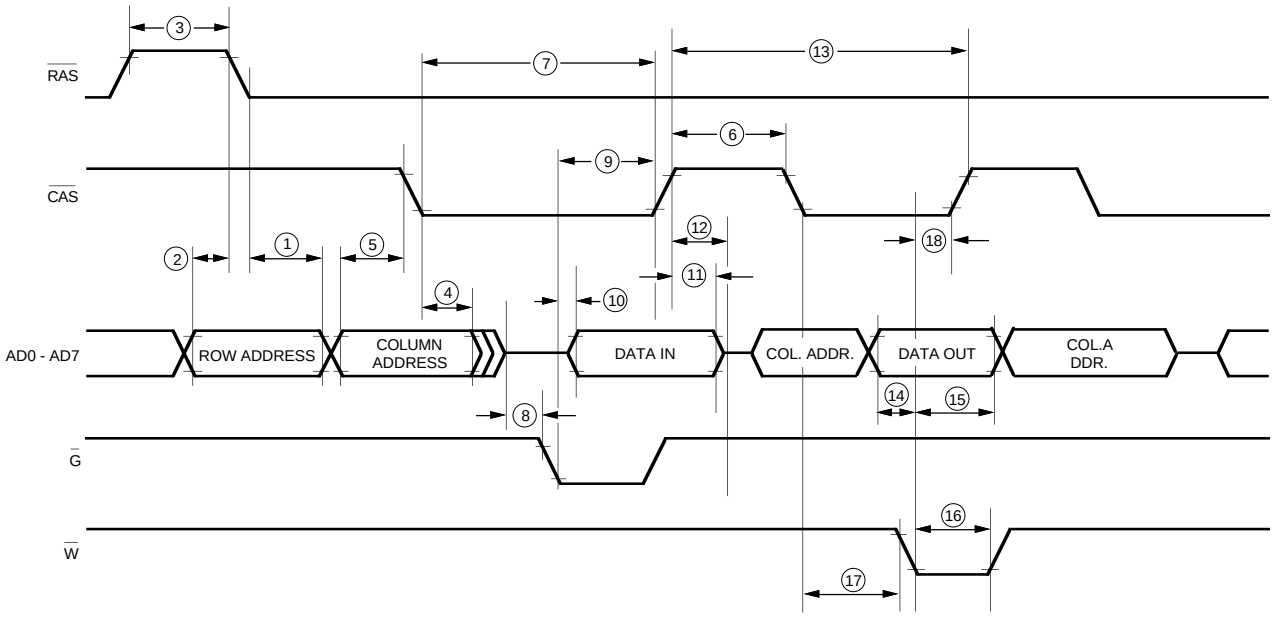


Figure E1. Local Dram Buffer Page-Mode Read and Write Cycle Timing Diagram

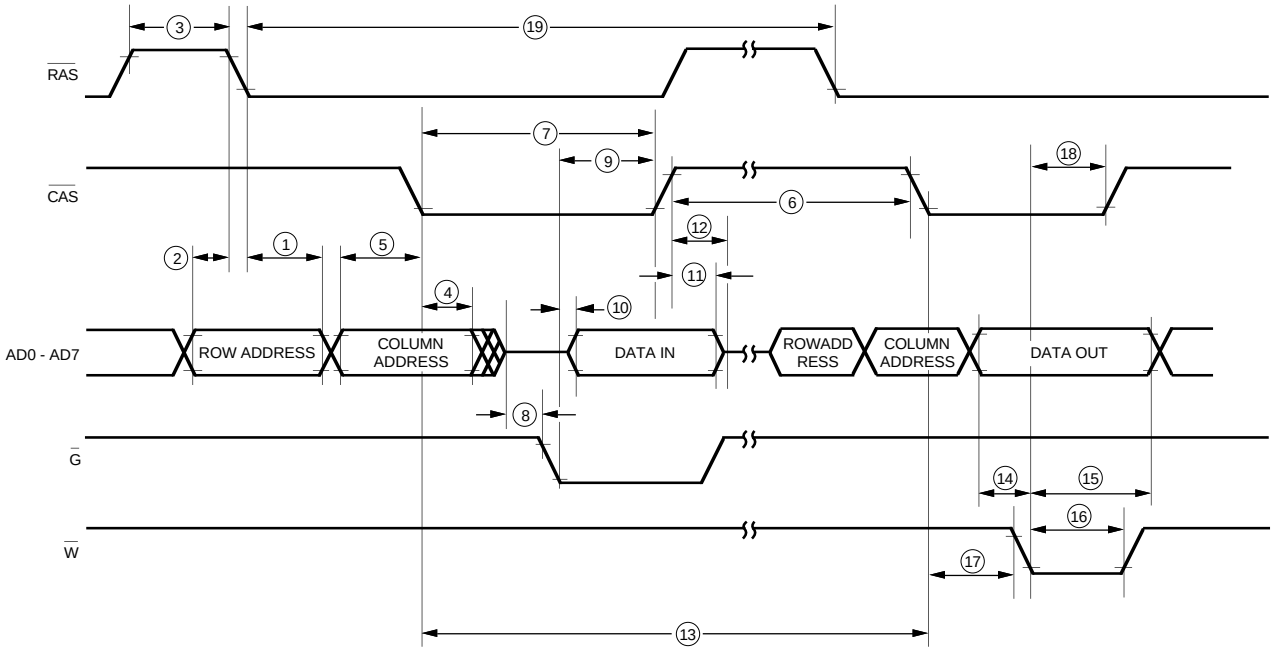


Figure E2. Local Dram Buffer Single Cycle Read and Write Cycle Timing Diagram

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{CC} range, unless otherwise specified)

Table F. Local Buffer Refresh Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVRSL	Address Setup Time to RAS*	25		ns
2	TRSLAX	Address Hold Time from RAS*	100		ns
3	TRSLRSH	RAS* Pulse Width	200		ns
4	TRSLRSL	RAS* Cycle Time	400		ns

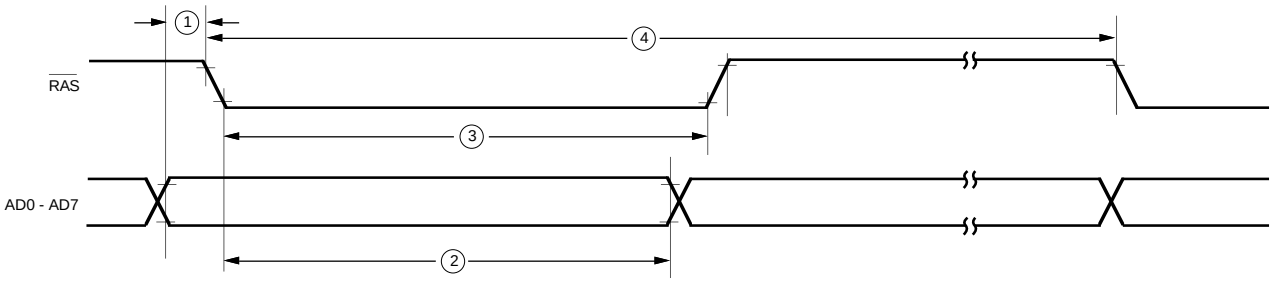


Figure F. Local Dram Buffer Refresh Cycle Timing Diagram

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{CC} range, unless otherwise specified)

Table G. Serial Interface Timing

Ref. #	Symbol	Description	Min.	Max.	Units
1	TCKHCKH	TXC*/RXC Cycle Time	100		ns
2	TCKHCKL	TXC*/RXC High Width	45		ns
3	TCKLCKH	TXC*/RXC Low Width	45		ns
4	TCKLDV	TXD Delay from TXC*		60	ns
5	TDVCKH	RXD Setup to RXC	30		ns
6	TCKHDX	RXD Hold Time from RXC	20		ns
7	TCKLTEH	TXEN Delay from TXC*		60	ns
8	TCKLTEL	TXEN Hold Time from TXC*	5		ns
9	TCSHCKH	CSN Setup to RXC	20		ns
10	TCKHCSL	CSN Hold Time from RXC	20		ns
11	TCHCL	COLL Pulse Width	200		ns

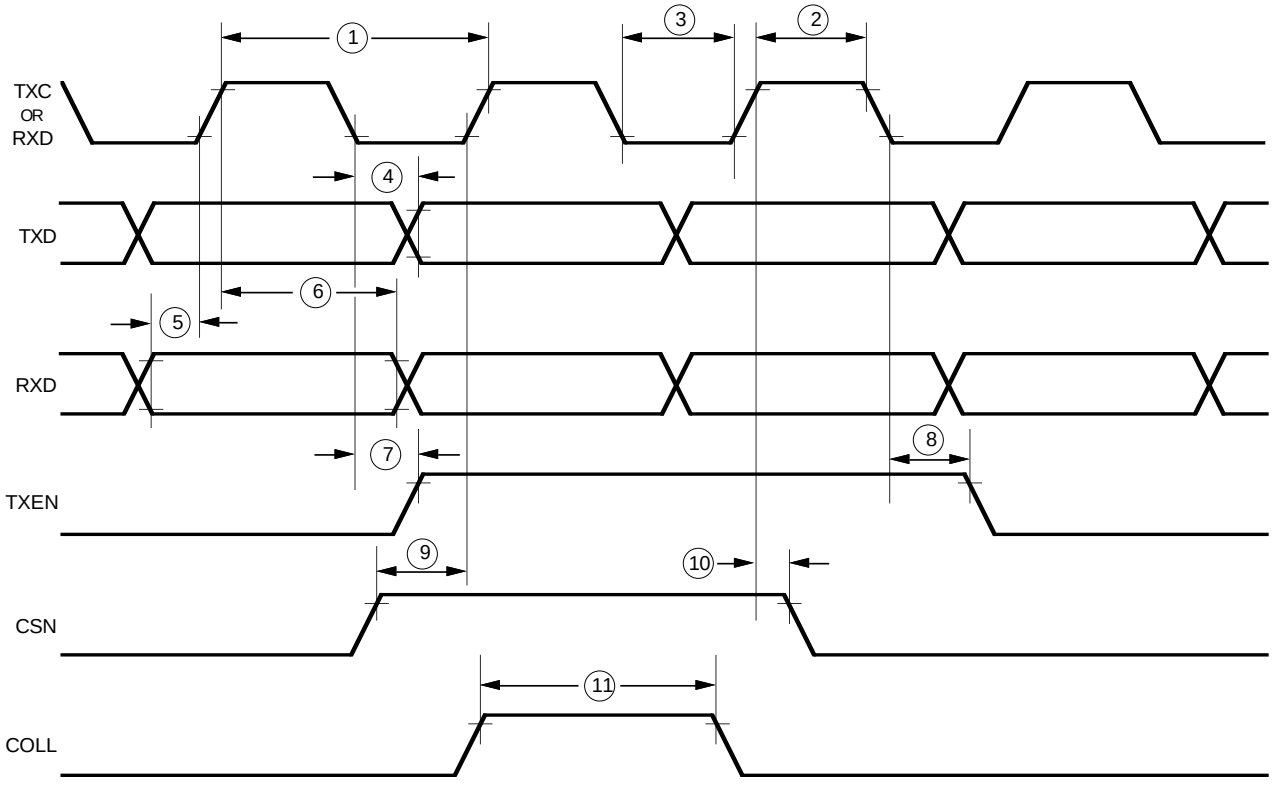


Figure G. Serial Transmit & Receive Interface Timing

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
(Over operating temperature and V_{CC} range, unless otherwise specified)

Table H. Master Clock and Reset Timing

Ref. #	Symbol	Description	Min.	Max.	Units
1	TCKHCKL	CLK Pulse Width High	15	25	ns
2	TCKLCKH	CLK Pulse Width Low	15	25	ns
3	TCKHCKH	CLK Cycle Time	49.9	50.1	ns
4	TRSLRSH	Reset Pulse Width	1		µs

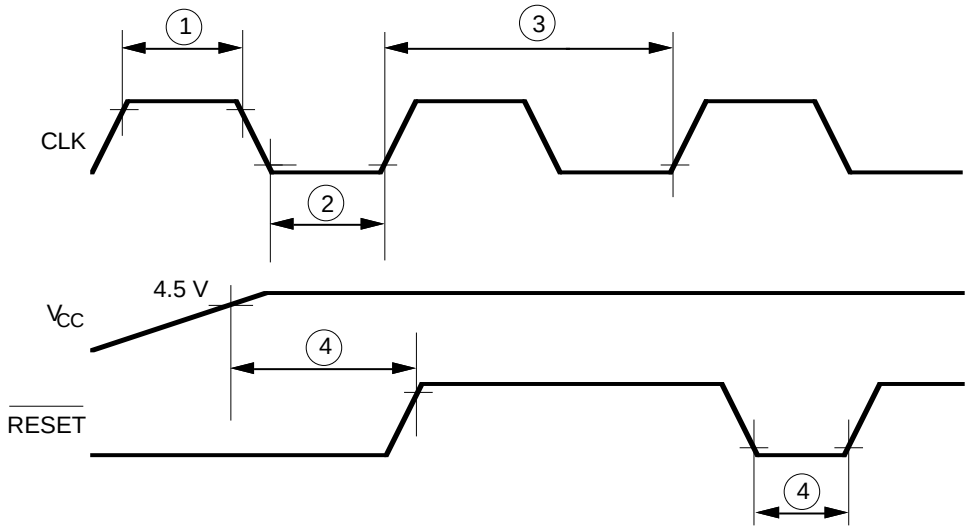


Figure H. Master Clock and Reset Timing

Ordering Information

PART NUMBER

N Q 80C04A

PRODUCT: 80C04A EDLC

TEMPERATURE RANGE: Q = 0° TO 70°C

PACKAGE TYPE: N = 68 PIN PLCC

NOTE: Please refer to App Note 33 8005/80C04 Design Guide, for additional information.