



PRODUCT BRIEF

Alpha 21264 Microprocessor

The Alpha 21264 microprocessor, with benchmarks over 30 SPECint95 and 50 SPECfp95, and with spectacular bandwidths over 3.2 GB/s for L2 cache and over 2.6 GB/s for memory, enables the system designer to produce the highest performance systems ranging from workstations to enterprise servers. Systems implemented with Alpha microprocessors have been the industry's performance leaders since their introduction in 1992.

Benefits

- Commercial Servers
 - A Scalable, High-Capacity, High-Bandwidth server to address business demands
 - Sustained Memory Bandwidth of over 1.6 GB/s
- Web Servers
 - Power for Real Time Compression/Decompression of Content
 - Bandwidth for Video Conferencing and Video Server
- Voice Computing Solution
 - Real-time Translator
 - 3D Human Interface and Visualizing Environment
- The 21264 provides end users with a quantum leap in performance for:
 - Real-time Visual Computing
 - Instant Data Mining
 - Internet Commerce Implementations
 - Enhanced Medical Imaging
 - DVD Authoring/Playback
 - Speech Recognition
 - Video Editing
- Alpha Motion-Video Instructions (MVI)
 - Optimizes Visual Computing (Video and 3D-Graphics)
 - Supports Real-time DVD Authoring (MPEG2 and AC-3)

Operating Systems

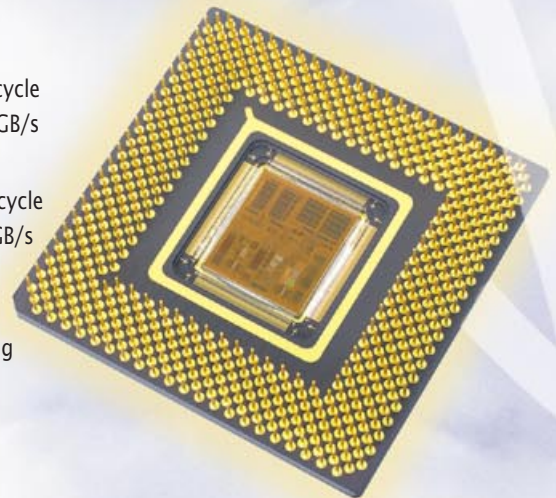
- Supports Windows NT
 - The first Windows NT 64-Bit platform.
 - Runs Non-Native Windows NT Applications using the DIGITAL FXI32 Binary Translator.
- Supports DIGITAL UNIX
 - The first 64-Bit UNIX operating system.
- Linux for Alpha
- Supports Alpha Open VMS

Description

The 21264 is the third-generation 64-Bit Alpha Microprocessor. It includes the latest Alpha architecture extensions, such as Motion-Video Instructions and Byte/Word operations.

The 21264 completely controls its L2 cache and provides flexible bus timing to support a range of L2 cache memory devices such as:

- 200MHz late-write SRAMs (3.2 GB/s)
- 166MHz (333MHz data rate) dual-data clock-forwarded SRAMs (5+ GB/s)
- L1 Cache: 2 64bit datapaths with 3 cycle load-to-use latency providing an 8+ GB/s Sustained Bandwidth
- L2 Bcache: 128bit datapath with 12 cycle load-to-use latency providing a 3.2 GB/s Sustained Bandwidth
- System Bus: 64bit datapath with 80 cycle load-to-use latency providing a 1.6 GB/s Sustained Bandwidth



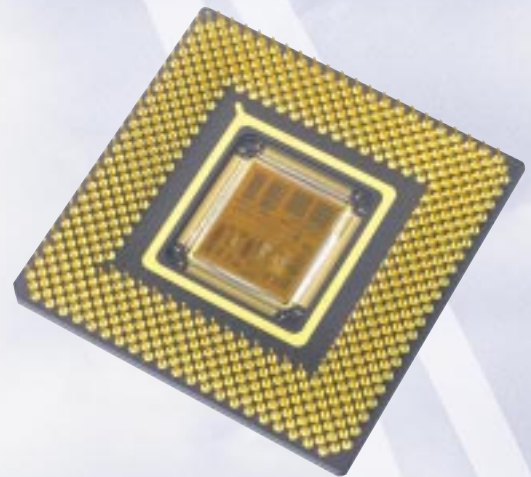
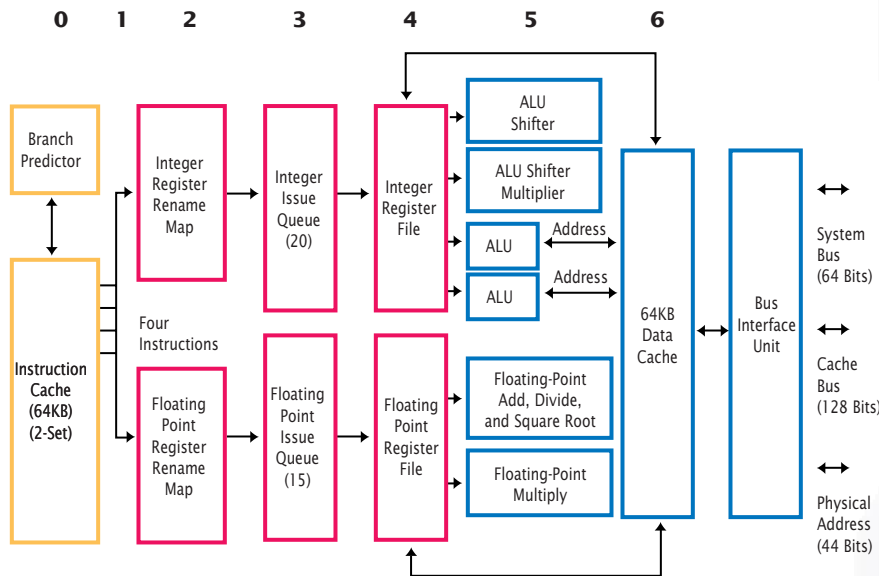
Pipeline Operation Sequence

The 21264 is a four-way out-of-order-issue microprocessor that performs dynamic scheduling, register renaming, and speculative execution. The 21264 pipeline contains four integer execution units. Two of the units can perform memory-address calculations for load and store operations. It also contains two floating-point execution units for add, divide, square root, and multiply functions.

The 21264 pipeline stages perform the following operations:

- Cycle 0 – Instruction fetch using branch prediction.
- Cycle 1 – Instruction data is transferred to the register rename map hardware.
- Cycle 2 – Rename (map) instruction registers.
- Cycle 3 – Issue instructions from the queues.
- Cycle 4 – Read instruction registers.
- Cycle 5 – Execute integer or floating-point instructions.
- Cycle 6 – Write results to Dcache or register.

The bus interface unit, containing the memory and cache control units, maintains coherency between the Dcache and the L2 cache and main memory.



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Power Supply Vss=0.0V, Vdd=2.1V min - 2.3V max

Operating Temperature Tj=100° C maximum (212° F)

Storage Temperature Range -55° C to + 125° C (-67° F to 257° F)

Package 587-pin CPGA

Transistor Count 15.2 million

Process 0.35 micron CMOS six-layer metal

Die Size Approximately 3.14 cm²

Availability February 1999

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